FIG.1

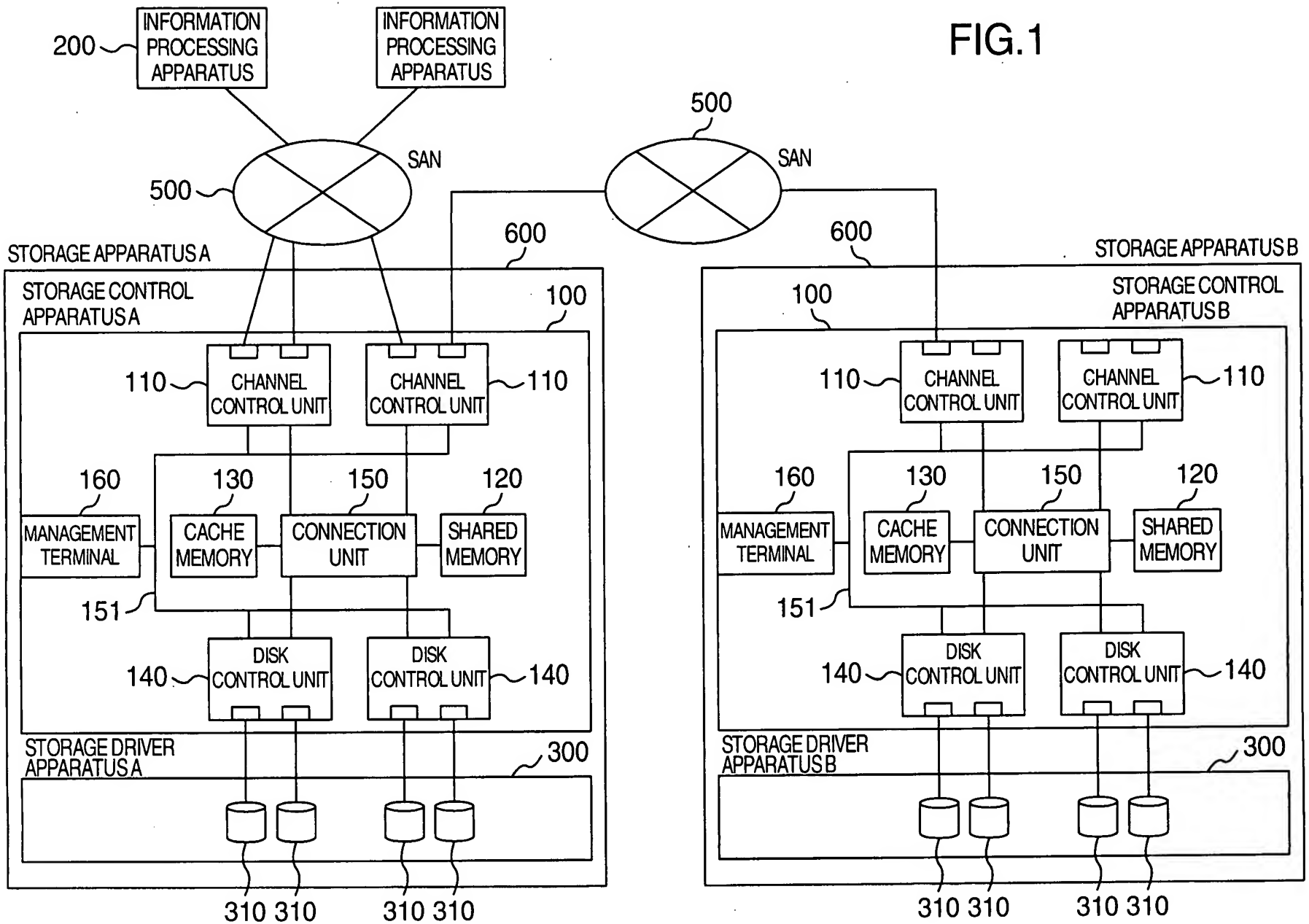

200
INFORMATION PROCESSING APPARATUS
INFORMATION PROCESSING APPARATUS
500
SAN
500
SAN
600
600
STORAGE APPARATUS A
STORAGE CONTROL APPARATUS A
100
110
CHANNEL CONTROL UNIT
CHANNEL CONTROL UNIT
110
160
130
150
120
MANAGEMENT TERMINAL
CACHE MEMORY
CONNECTION UNIT
SHARED MEMORY
151
140
DISK CONTROL UNIT
DISK CONTROL UNIT
140
STORAGE DRIVER APPARATUS A
300
310 310
310 310
STORAGE APPARATUS B
STORAGE CONTROL APPARATUS B
100
110
CHANNEL CONTROL UNIT
CHANNEL CONTROL UNIT
110
160
130
150
120
MANAGEMENT TERMINAL
CACHE MEMORY
CONNECTION UNIT
SHARED MEMORY
151
140
DISK CONTROL UNIT
DISK CONTROL UNIT
140
STORAGE DRIVER APPARATUS B
300
310 310
310 310

FIG.2

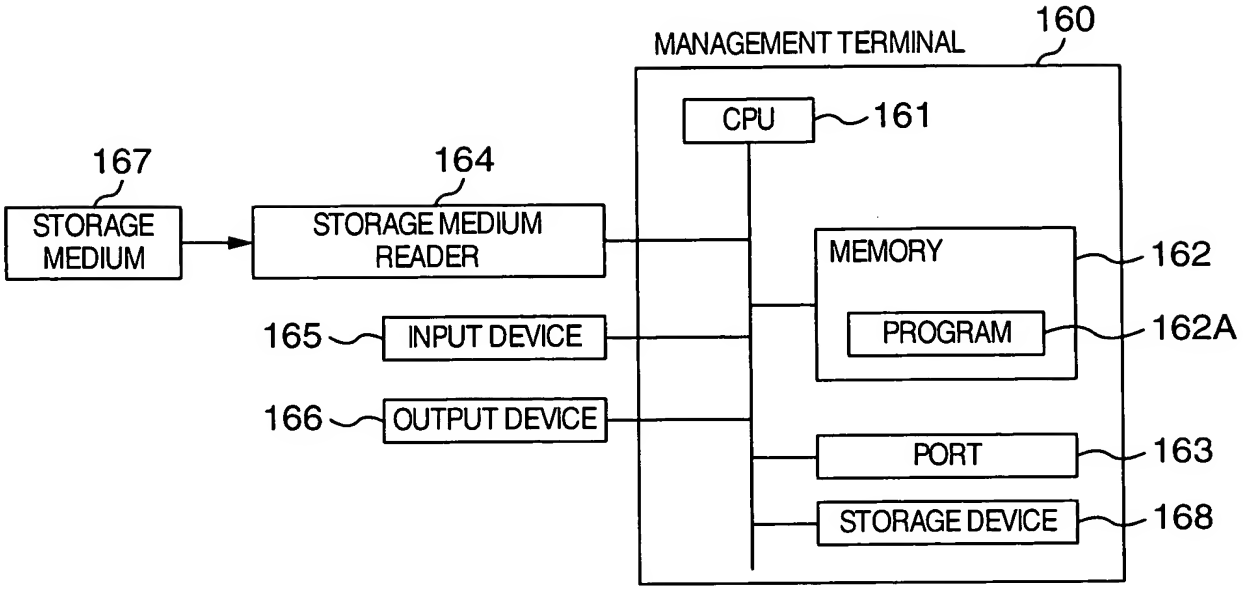

MANAGEMENT TERMINAL
160
CPU
161
167
164
STORAGE MEDIUM
STORAGE MEDIUM READER
MEMORY
162
PROGRAM
162A
165
INPUT DEVICE
166
OUTPUT DEVICE
PORT
163
STORAGE DEVICE
168

FIG.3

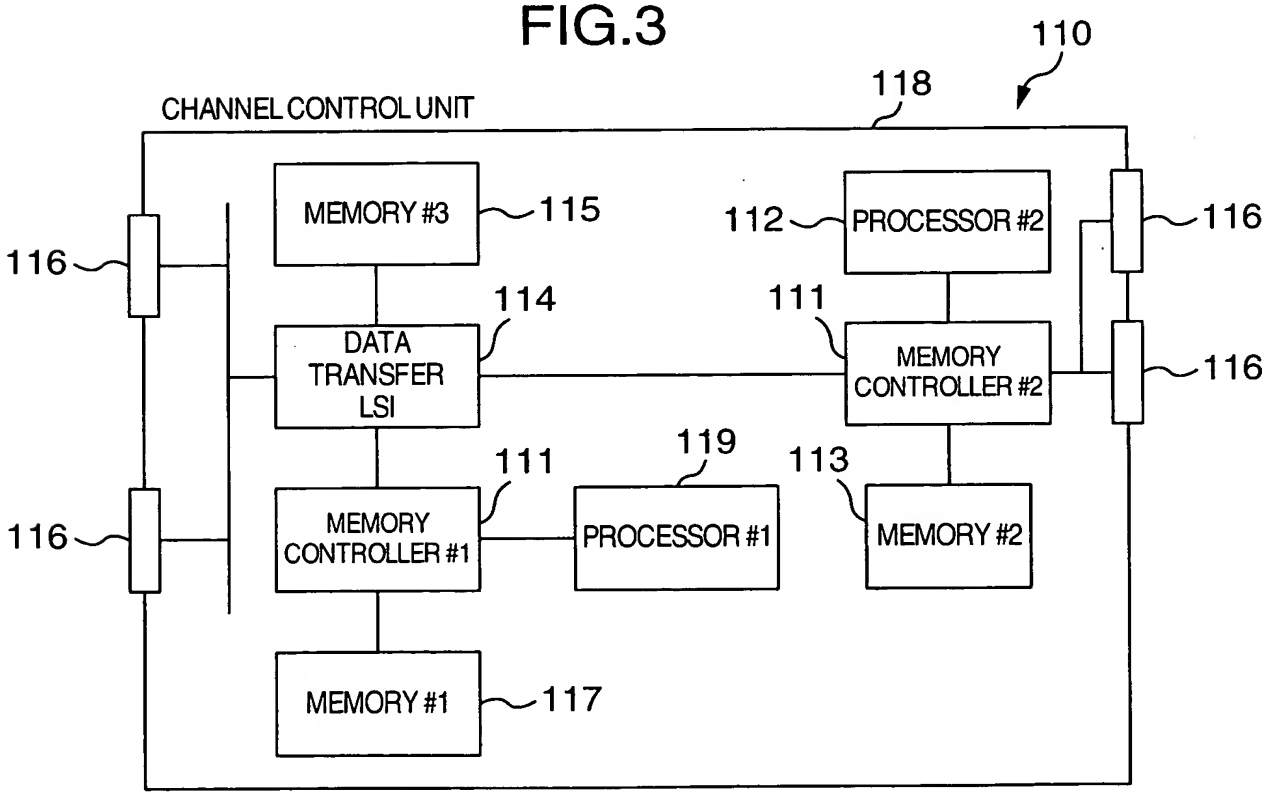

110
118
CHANNEL CONTROL UNIT
MEMORY #3
115
112
PROCESSOR #2
116
116
114
111
DATA TRANSFER LSI
MEMORY CONTROLLER #2
116
111
119
113
116
MEMORY CONTROLLER #1
PROCESSOR #1
MEMORY #2
MEMORY #1
117

FIG.4

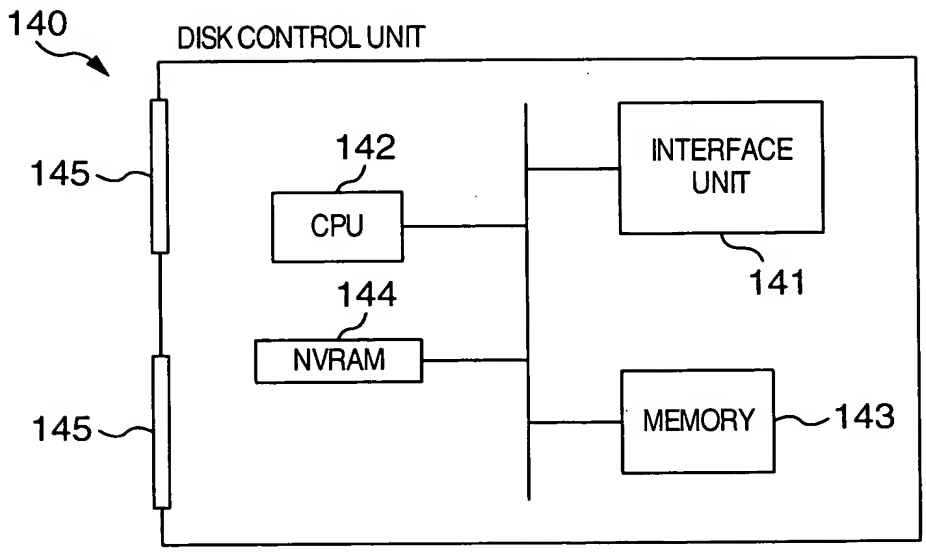

140
DISK CONTROL UNIT
145
142
CPU
144
NVRAM
145
INTERFACE UNIT
141
MEMORY
143

FIG.5

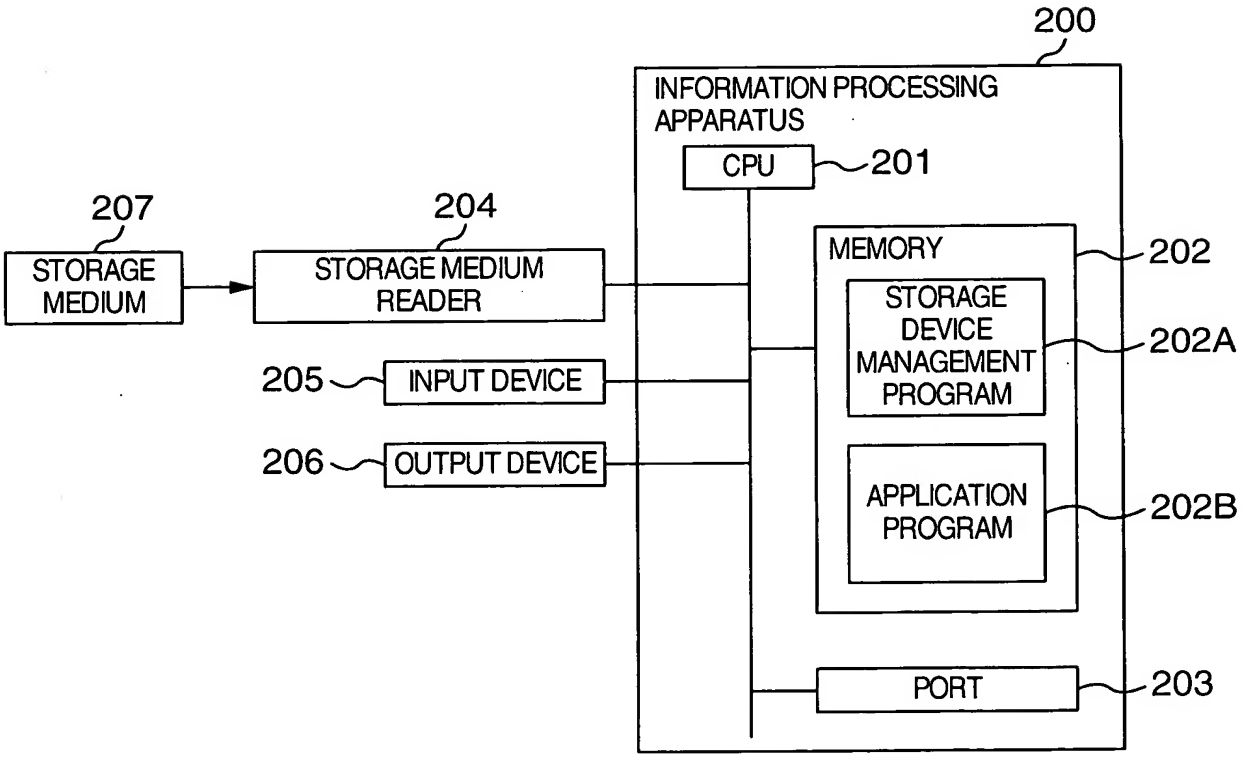

200
INFORMATION PROCESSING APPARATUS
CPU
201
207
STORAGE MEDIUM
204
STORAGE MEDIUM READER
205
INPUT DEVICE
206
OUTPUT DEVICE
MEMORY
202
STORAGE DEVICE MANAGEMENT PROGRAM
202A
APPLICATION PROGRAM
202B
PORT
203

FIG.6

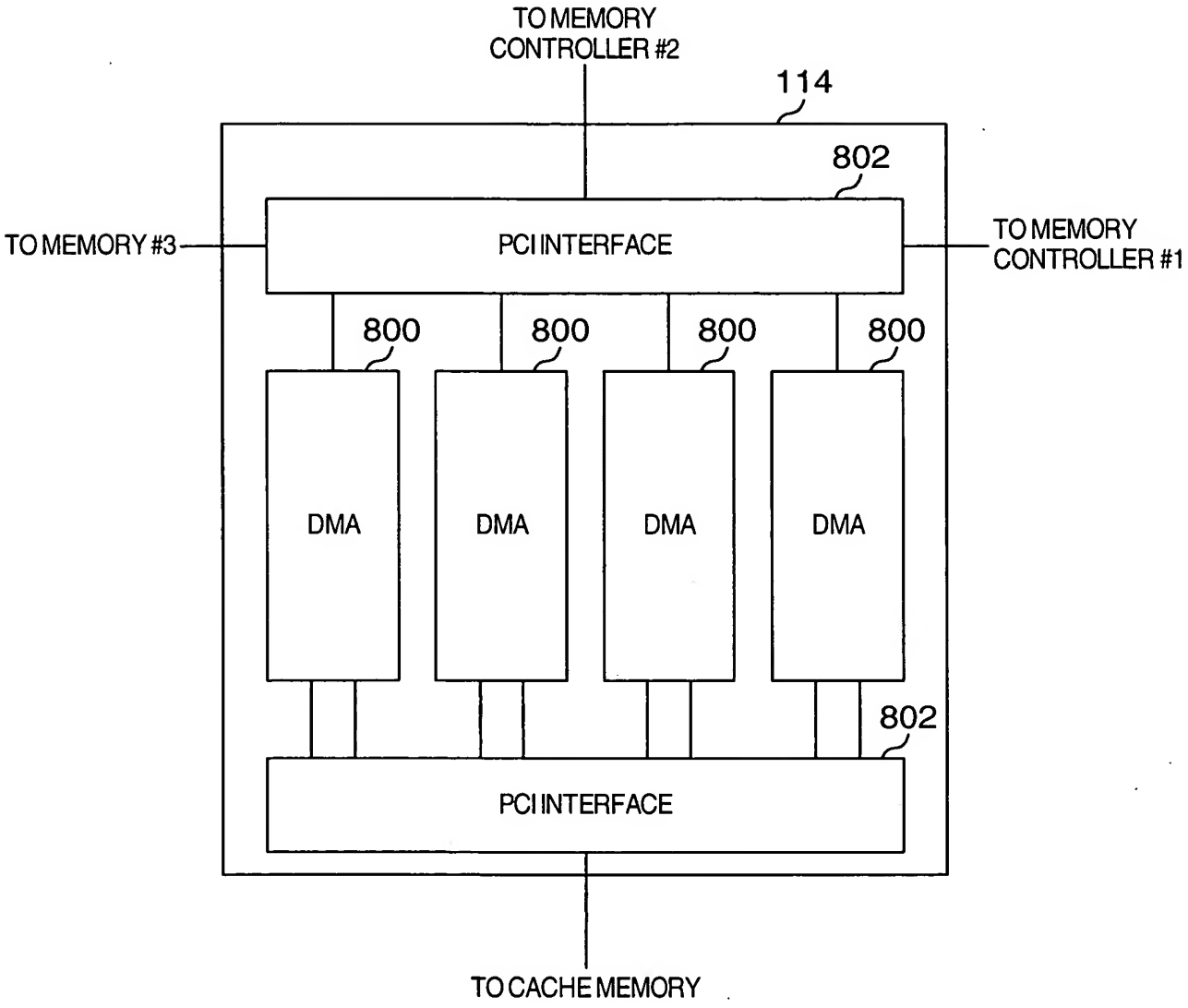

TO MEMORY CONTROLLER #2
114
802
TO MEMORY #3
PCI INTERFACE
TO MEMORY CONTROLLER #1
800
800
800
800
DMA
DMA
DMA
DMA
802
PCI INTERFACE
TO CACHE MEMORY

FIG.7

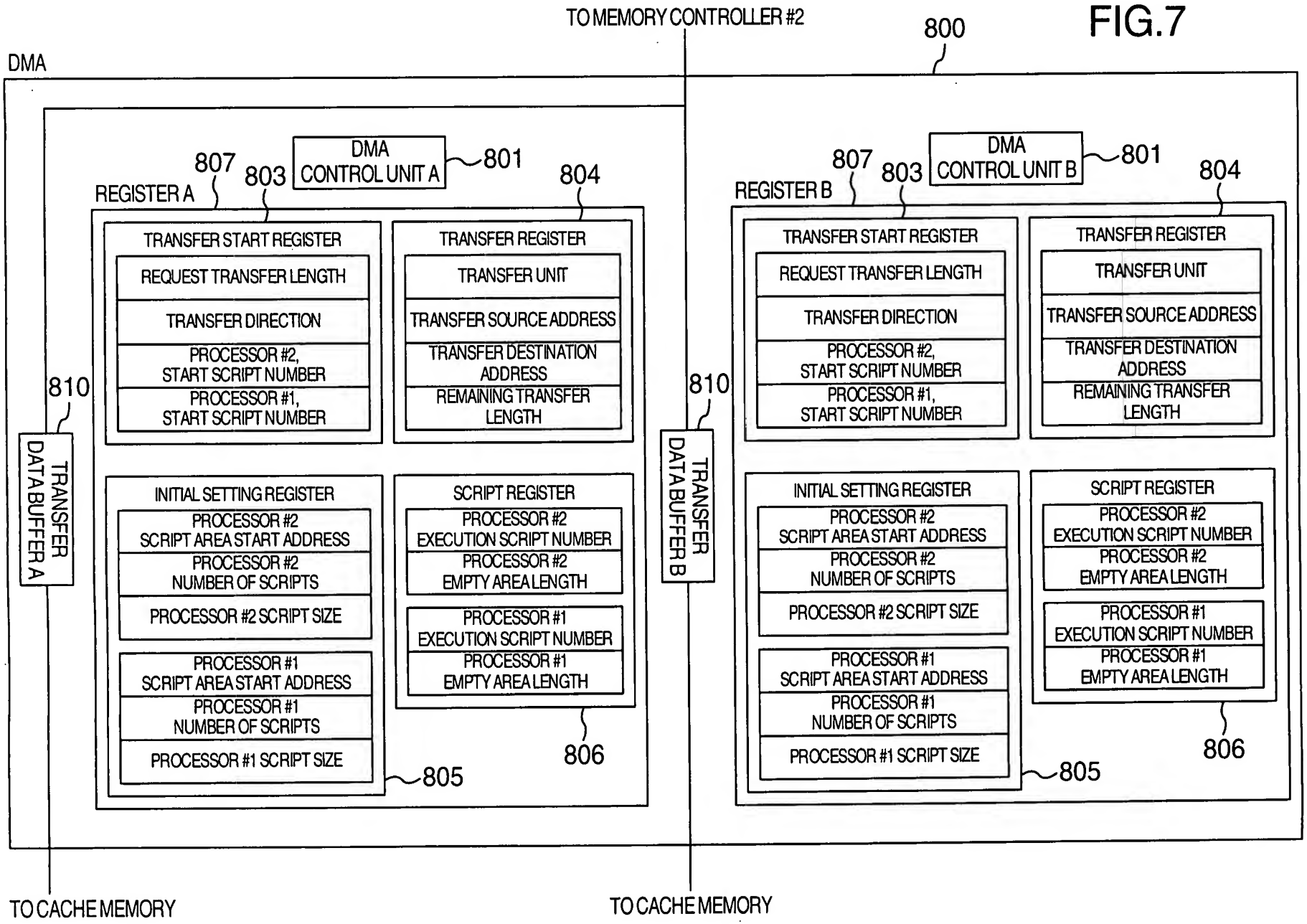

TO MEMORY CONTROLLER #2
800
DMA
807
803
DMA CONTROL UNIT A
801
804
REGISTER A
TRANSFER START REGISTER
REQUEST TRANSFER LENGTH
TRANSFER DIRECTION
PROCESSOR #2, START SCRIPT NUMBER
PROCESSOR #1, START SCRIPT NUMBER
TRANSFER REGISTER
TRANSFER UNIT
TRANSFER SOURCE ADDRESS
TRANSFER DESTINATION ADDRESS
REMAINING TRANSFER LENGTH
810
TRANSFER DATA BUFFER A
INITIAL SETTING REGISTER
PROCESSOR #2 SCRIPT AREA START ADDRESS
PROCESSOR #2 NUMBER OF SCRIPTS
PROCESSOR #2 SCRIPT SIZE
PROCESSOR #1 SCRIPT AREA START ADDRESS
PROCESSOR #1 NUMBER OF SCRIPTS
PROCESSOR #1 SCRIPT SIZE
805
SCRIPT REGISTER
PROCESSOR #2 EXECUTION SCRIPT NUMBER
PROCESSOR #2 EMPTY AREA LENGTH
PROCESSOR #1 EXECUTION SCRIPT NUMBER
PROCESSOR #1 EMPTY AREA LENGTH
806
807
803
DMA CONTROL UNIT B
801
804
REGISTER B
TRANSFER START REGISTER
REQUEST TRANSFER LENGTH
TRANSFER DIRECTION
PROCESSOR #2, START SCRIPT NUMBER
PROCESSOR #1, START SCRIPT NUMBER
TRANSFER REGISTER
TRANSFER UNIT
TRANSFER SOURCE ADDRESS
TRANSFER DESTINATION ADDRESS
REMAINING TRANSFER LENGTH
810
TRANSFER DATA BUFFER B
INITIAL SETTING REGISTER
PROCESSOR #2 SCRIPT AREA START ADDRESS
PROCESSOR #2 NUMBER OF SCRIPTS
PROCESSOR #2 SCRIPT SIZE
PROCESSOR #1 SCRIPT AREA START ADDRESS
PROCESSOR #1 NUMBER OF SCRIPTS
PROCESSOR #1 SCRIPT SIZE
805
SCRIPT REGISTER
PROCESSOR #2 EXECUTION SCRIPT NUMBER
PROCESSOR #2 EMPTY AREA LENGTH
PROCESSOR #1 EXECUTION SCRIPT NUMBER
PROCESSOR #1 EMPTY AREA LENGTH
806
TO CACHE MEMORY
TO CACHE MEMORY

FIG.8

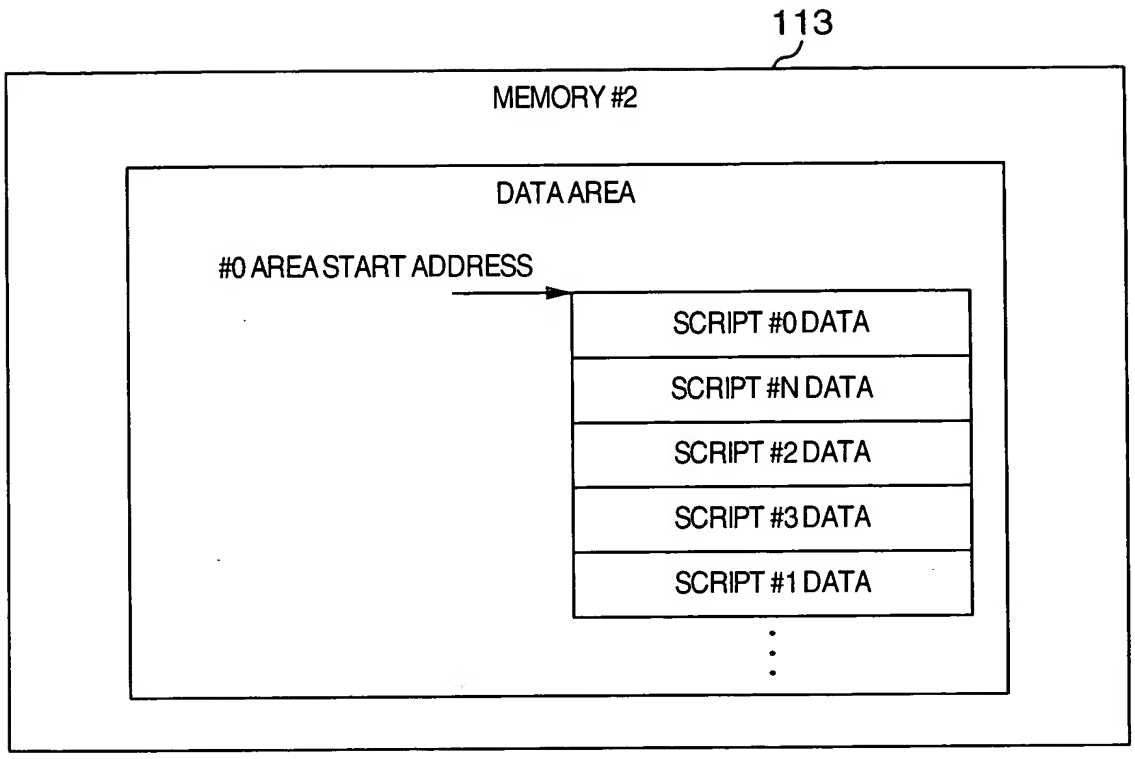

113
MEMORY #2
DATA AREA
#0 AREA START ADDRESS
SCRIPT #0 DATA
SCRIPT #N DATA
SCRIPT #2 DATA
SCRIPT #3 DATA
SCRIPT #1 DATA

FIG.9

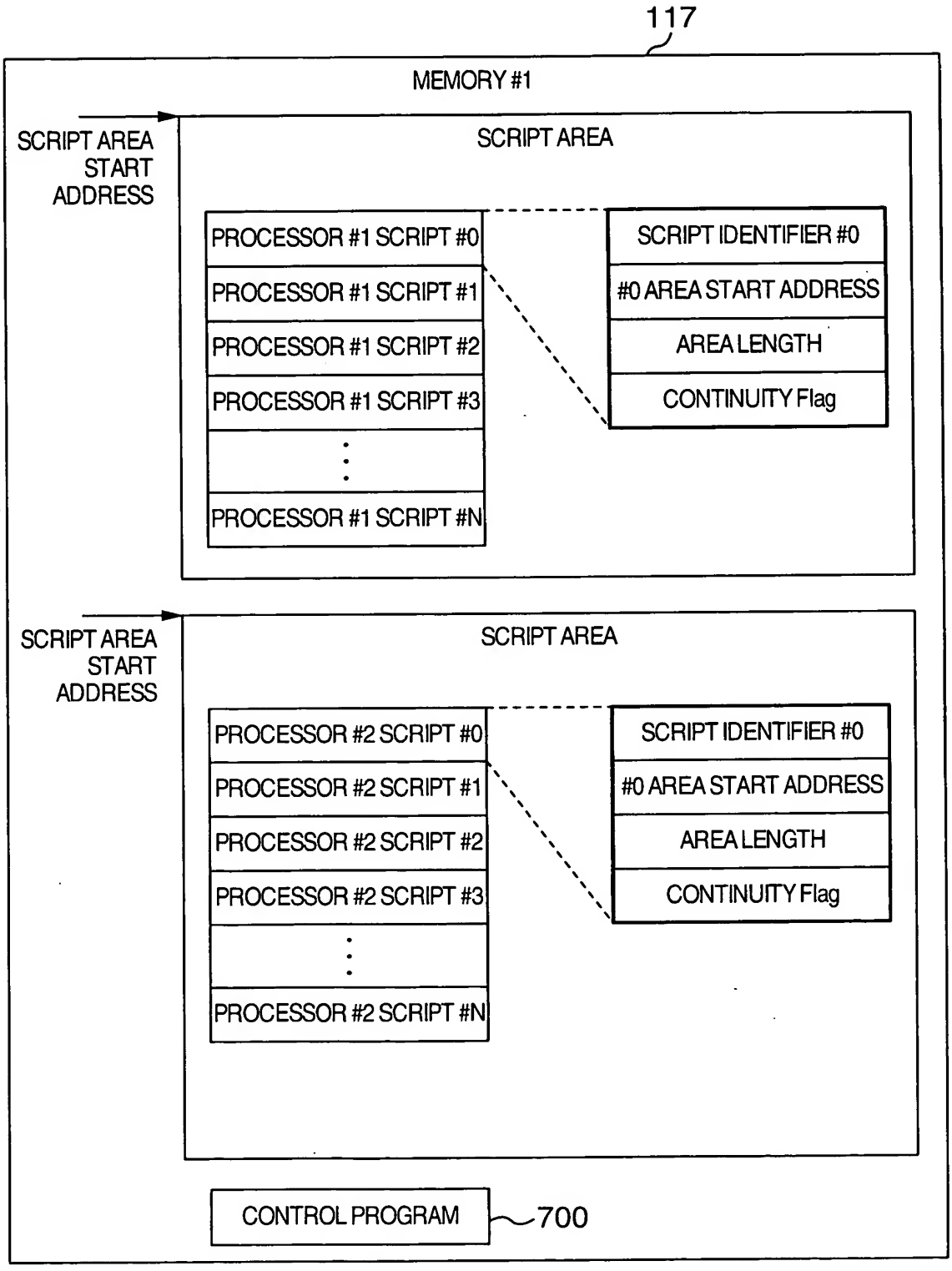

117
MEMORY #1
SCRIPT AREA START ADDRESS
SCRIPT AREA
PROCESSOR #1 SCRIPT #0
PROCESSOR #1 SCRIPT #1
PROCESSOR #1 SCRIPT #2
PROCESSOR #1 SCRIPT #3
PROCESSOR #1 SCRIPT #N
SCRIPT IDENTIFIER #0
#0 AREA START ADDRESS
AREA LENGTH
CONTINUITY Flag
SCRIPT AREA START ADDRESS
SCRIPT AREA
PROCESSOR #2 SCRIPT #0
PROCESSOR #2 SCRIPT #1
PROCESSOR #2 SCRIPT #2
PROCESSOR #2 SCRIPT #3
PROCESSOR #2 SCRIPT #N
SCRIPT IDENTIFIER #0
#0 AREA START ADDRESS
AREA LENGTH
CONTINUITY Flag
CONTROL PROGRAM
700

FIG.10

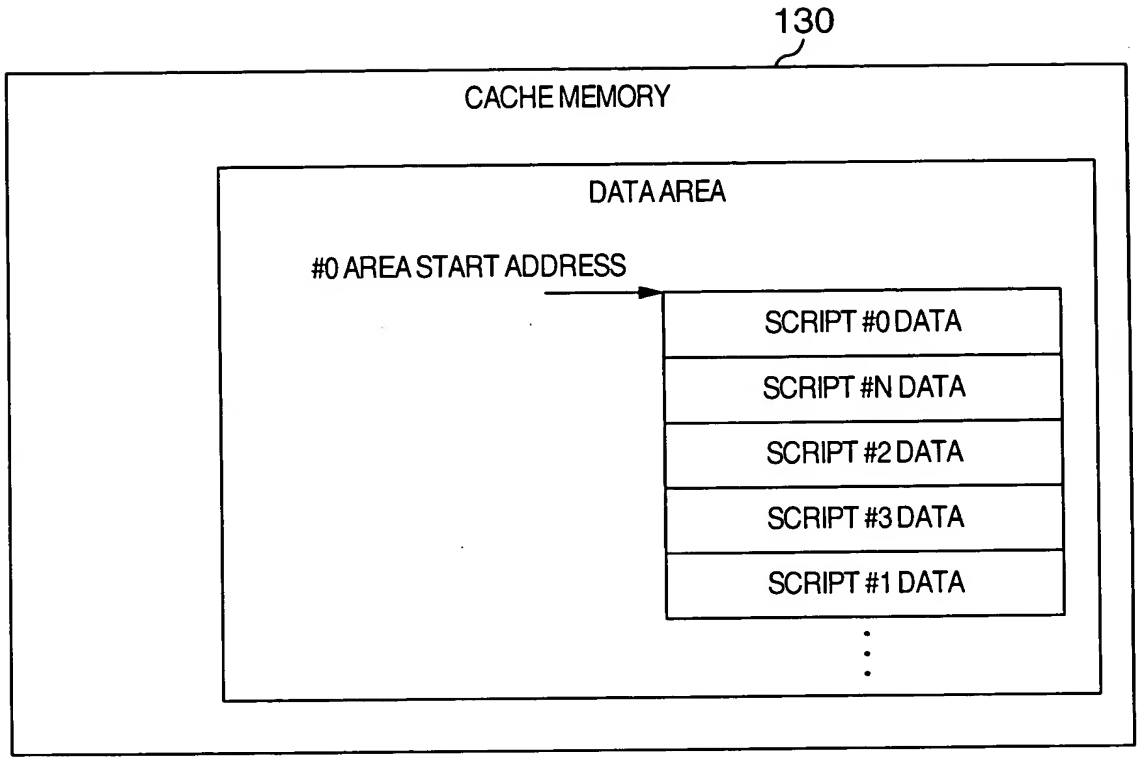

130
CACHE MEMORY
DATA AREA
#0 AREA START ADDRESS
SCRIPT #0 DATA
SCRIPT #N DATA
SCRIPT #2 DATA
SCRIPT #3 DATA
SCRIPT #1 DATA

FIG.11

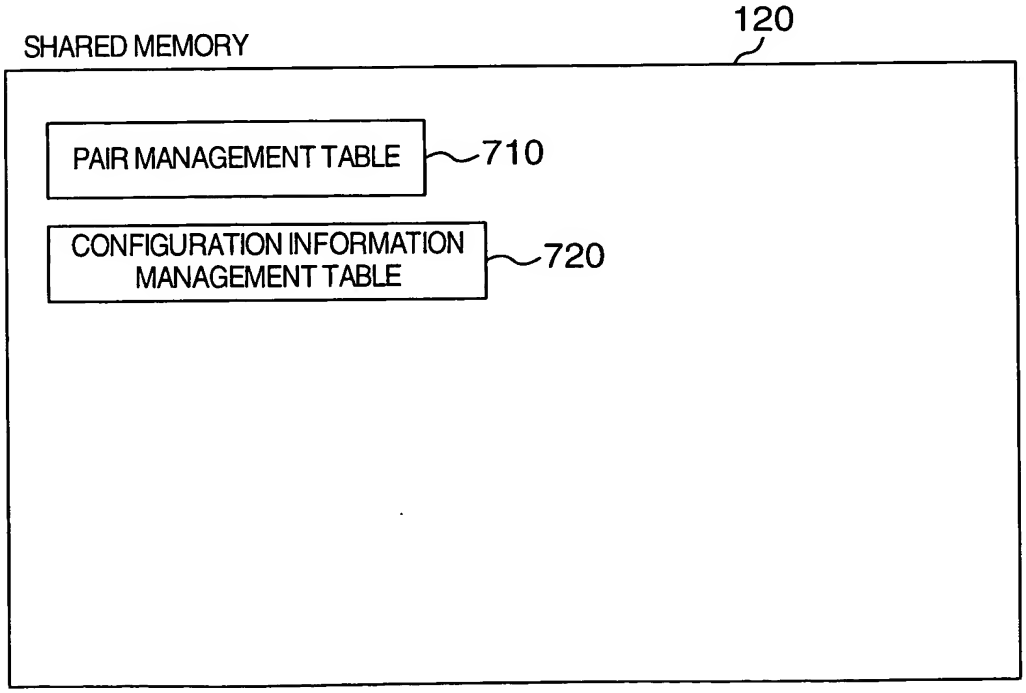

120
SHARED MEMORY
PAIR MANAGEMENT TABLE
710
CONFIGURATION INFORMATION MANAGEMENT TABLE
720

FIG.12

710

PAIR MANAGEMENT TABLE

PAIR TYPE	COPY TYPE	COPY SOURCE APPARATUS	COPY DESTINATION APPARATUS	COPY SOURCE VOLUME	COPY DESTINATION VOLUME	PAIR STATE
LOCAL	—	—	—	0	2	IN PAIR
LOCAL	—	—	—	1	3	IN PAIR
REMOTE	ASYNCHRONOUS	A	B	0	0	IN SPLIT
⋮	⋮	⋮	⋮	⋮	⋮	⋮

FIG.13

720

Port ID	WWN	LUN	Capacity (KB)	MAPPING LUN
010001	XXZZYYXX00002141	3	3,072	01:03
010006	ad00bbffzz00a1ffd	5	5,120	3B:20
⋮	⋮	⋮	⋮	⋮
032F31	XXZZYYXX00002142	2	45,897	02:01

FIG.14

730

HOST ID	PORT ID	LUN	ADDRESS	DATA LENGTH

FIG.15

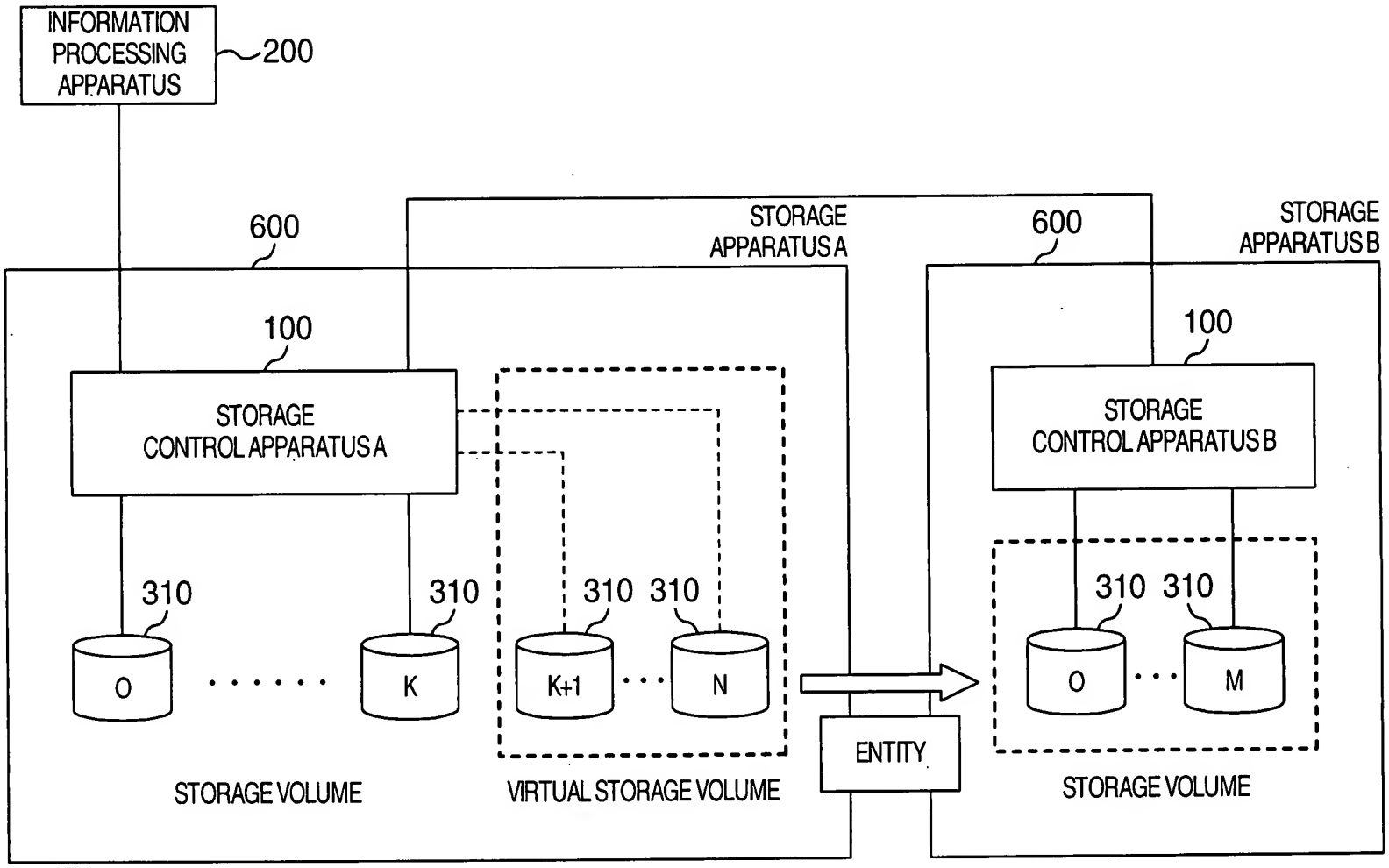

INFORMATION PROCESSING APPARATUS
200
600
STORAGE APPARATUS A
600
STORAGE APPARATUS B
100
100
STORAGE CONTROL APPARATUS A
STORAGE CONTROL APPARATUS B
310
310
310
310
310
310
0
K
K+1
N
0
M
ENTITY
STORAGE VOLUME
VIRTUAL STORAGE VOLUME
STORAGE VOLUME

FIG.16

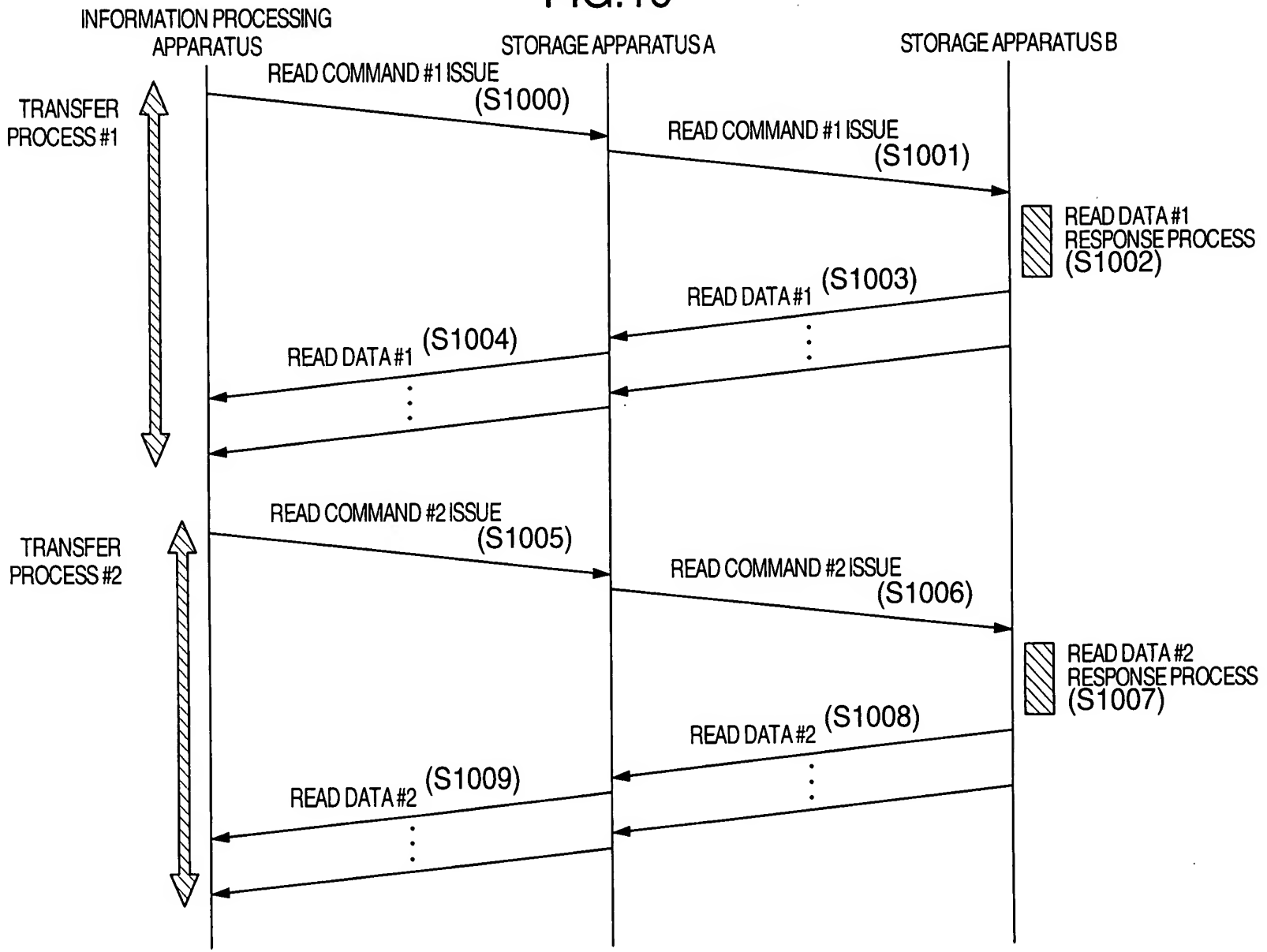

INFORMATION PROCESSING APPARATUS
STORAGE APPARATUS A
STORAGE APPARATUS B
TRANSFER PROCESS #1
READ COMMAND #1 ISSUE (S1000)
READ COMMAND #1 ISSUE (S1001)
READ DATA #1 RESPONSE PROCESS (S1002)
READ DATA #1 (S1003)
READ DATA #1 (S1004)
TRANSFER PROCESS #2
READ COMMAND #2 ISSUE (S1005)
READ COMMAND #2 ISSUE (S1006)
READ DATA #2 RESPONSE PROCESS (S1007)
READ DATA #2 (S1008)
READ DATA #2 (S1009)

FIG.17

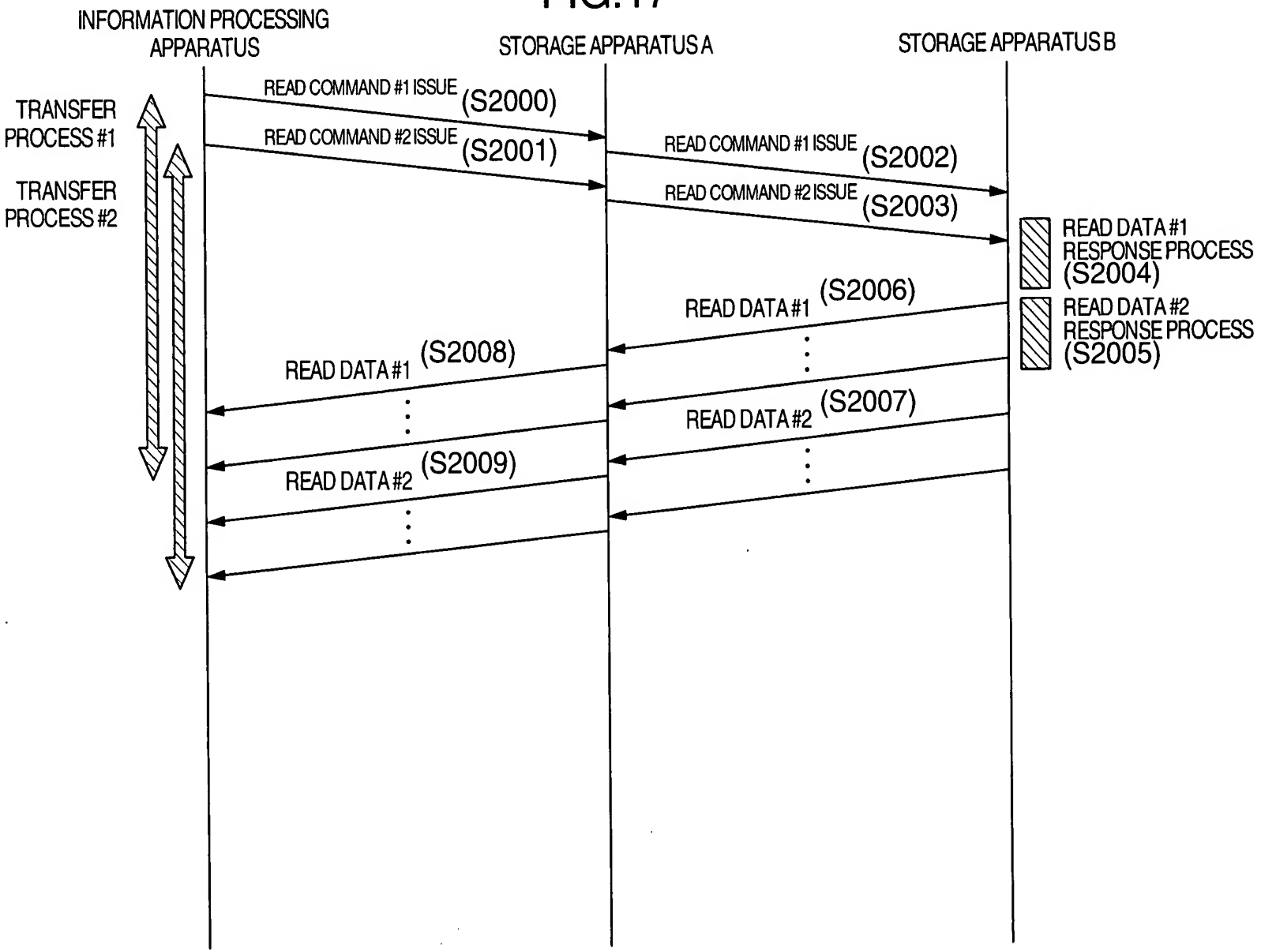

INFORMATION PROCESSING APPARATUS
STORAGE APPARATUS A
STORAGE APPARATUS B
TRANSFER PROCESS #1
TRANSFER PROCESS #2
READ COMMAND #1 ISSUE (S2000)
READ COMMAND #2 ISSUE (S2001)
READ COMMAND #1 ISSUE (S2002)
READ COMMAND #2 ISSUE (S2003)
READ DATA #1 RESPONSE PROCESS (S2004)
READ DATA #2 RESPONSE PROCESS (S2005)
READ DATA #1 (S2006)
READ DATA #2 (S2007)
READ DATA #1 (S2008)
READ DATA #2 (S2009)

FIG.18

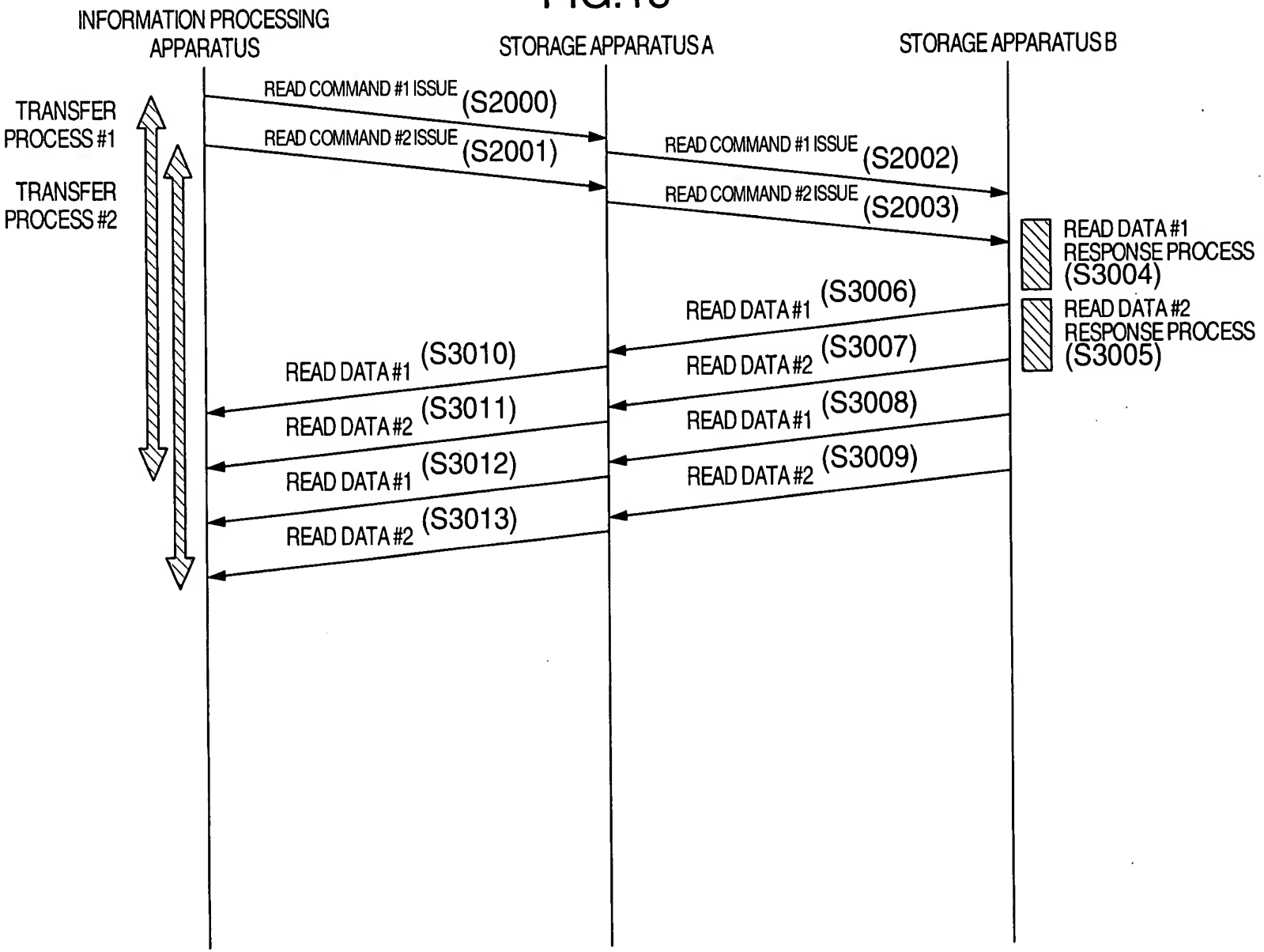

INFORMATION PROCESSING APPARATUS
STORAGE APPARATUS A
STORAGE APPARATUS B
TRANSFER PROCESS #1
TRANSFER PROCESS #2
READ COMMAND #1 ISSUE (S2000)
READ COMMAND #2 ISSUE (S2001)
READ COMMAND #1 ISSUE (S2002)
READ COMMAND #2 ISSUE (S2003)
READ DATA #1 RESPONSE PROCESS (S3004)
READ DATA #2 RESPONSE PROCESS (S3005)
READ DATA #1 (S3006)
READ DATA #2 (S3007)
READ DATA #1 (S3008)
READ DATA #2 (S3009)
READ DATA #1 (S3010)
READ DATA #2 (S3011)
READ DATA #1 (S3012)
READ DATA #2 (S3013)

FIG.19

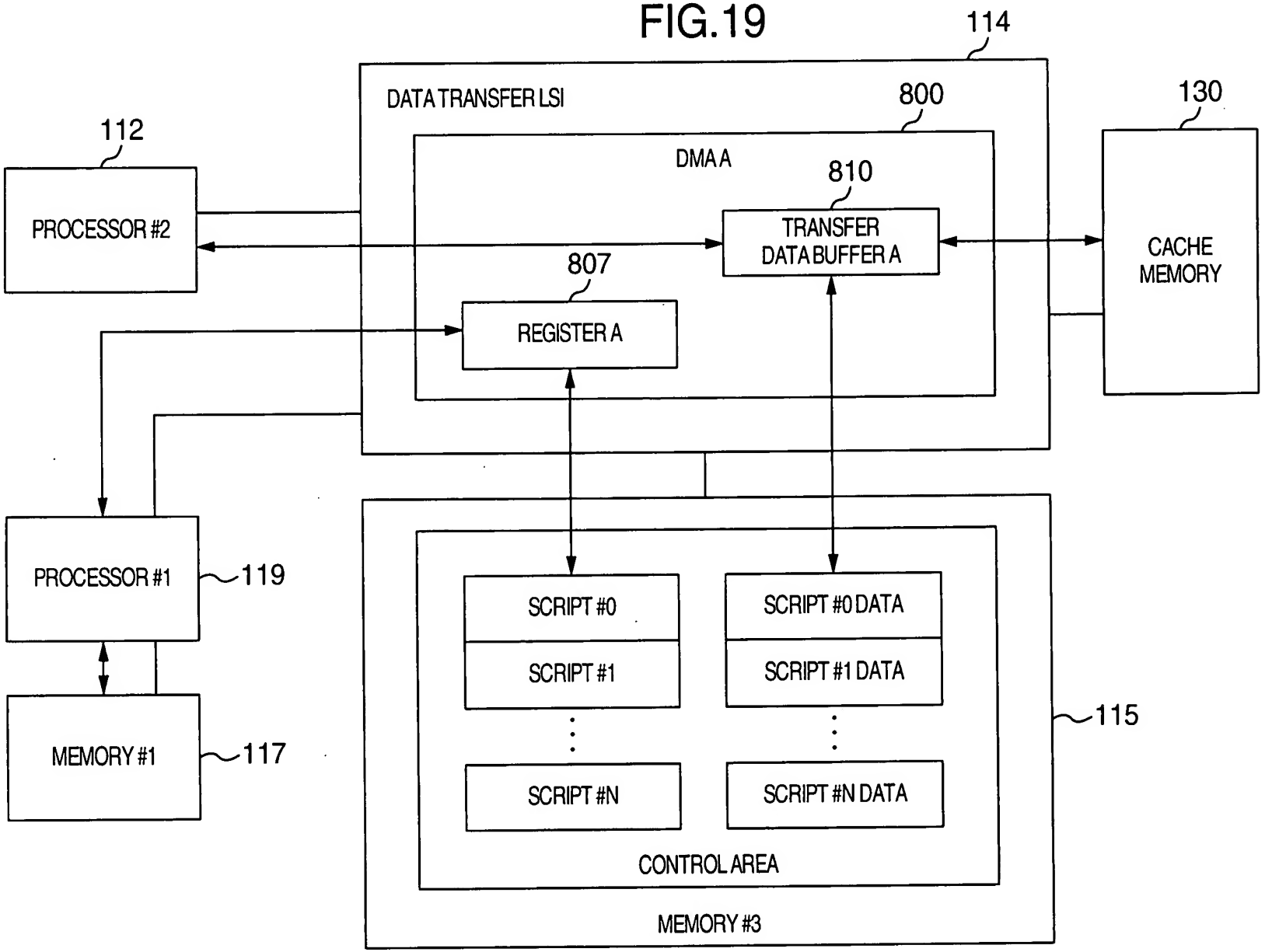

114
DATA TRANSFER LSI
800
130
112
DMA A
810
PROCESSOR #2
TRANSFER DATA BUFFER A
CACHE MEMORY
807
REGISTER A
PROCESSOR #1
119
SCRIPT #0
SCRIPT #0 DATA
SCRIPT #1
SCRIPT #1 DATA
115
MEMORY #1
117
SCRIPT #N
SCRIPT #N DATA
CONTROL AREA
MEMORY #3

FIG.20

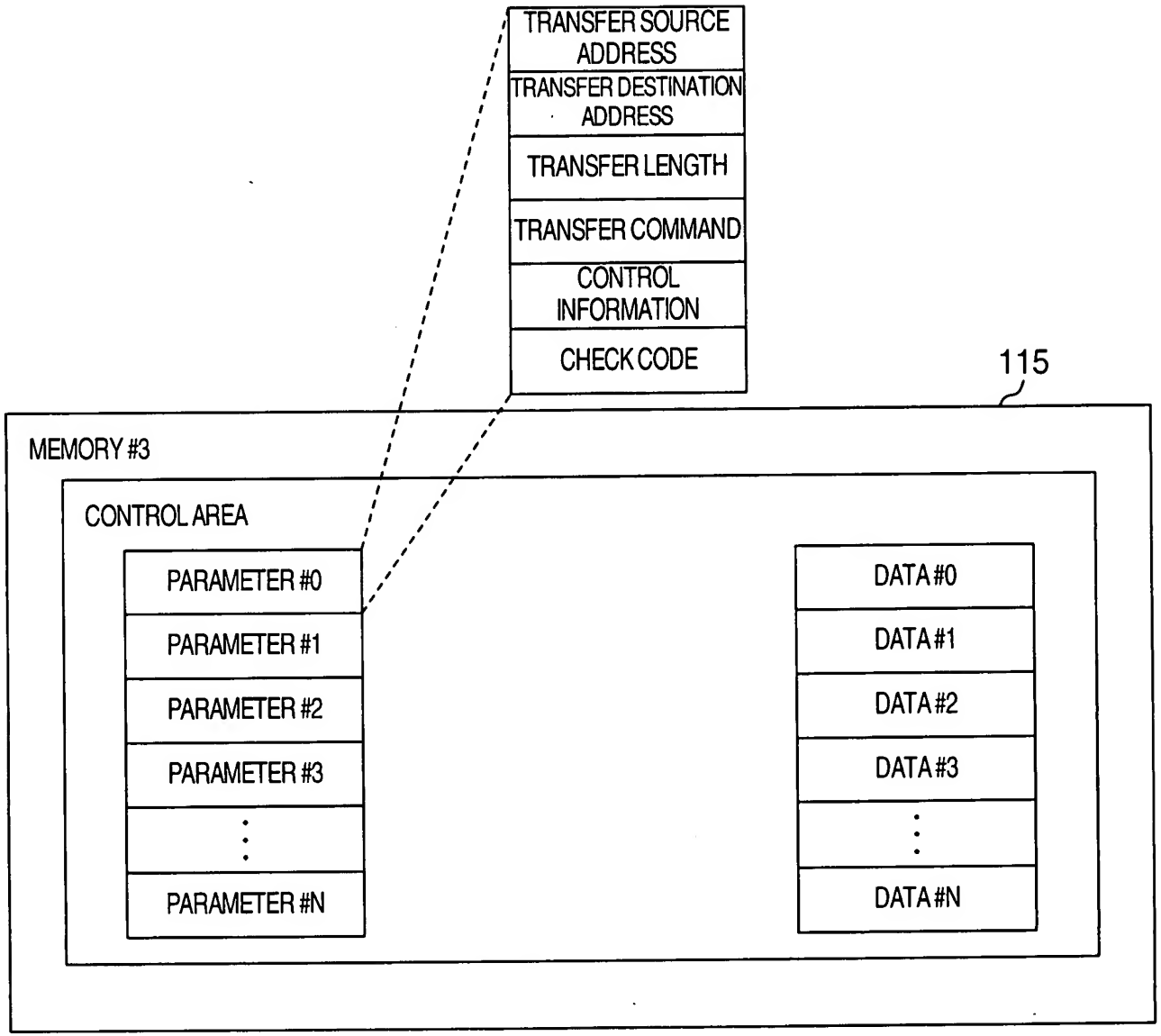

TRANSFER SOURCE ADDRESS
TRANSFER DESTINATION ADDRESS
TRANSFER LENGTH
TRANSFER COMMAND
CONTROL INFORMATION
CHECK CODE
115
MEMORY #3
CONTROL AREA
PARAMETER #0
PARAMETER #1
PARAMETER #2
PARAMETER #3
PARAMETER #N
DATA #0
DATA #1
DATA #2
DATA #3
DATA #N

FIG.21

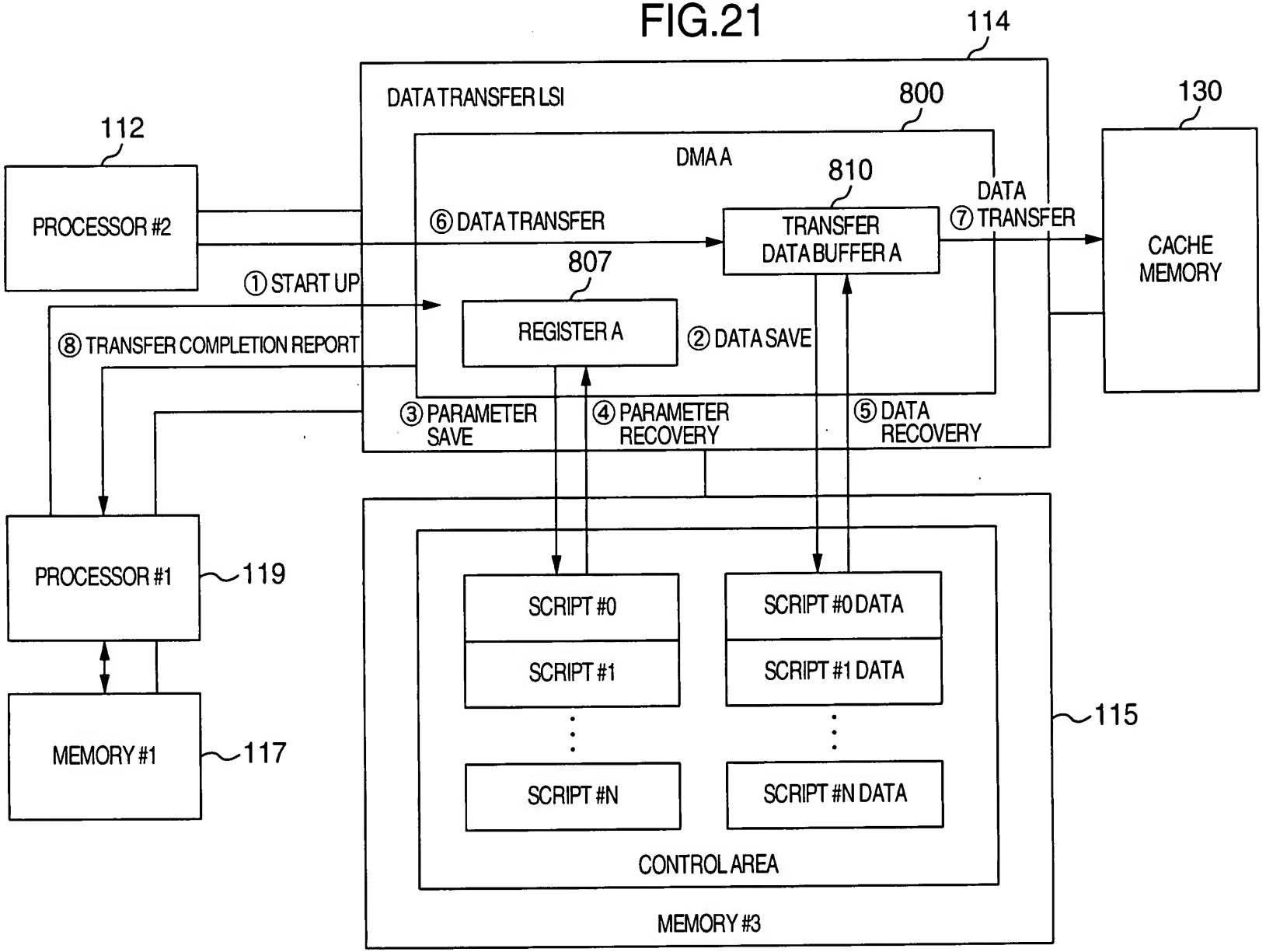

114
DATA TRANSFER LSI
800
130
112
DMA A
810
PROCESSOR #2
⑥ DATA TRANSFER
TRANSFER DATA BUFFER A
DATA ⑦ TRANSFER
CACHE MEMORY
807
① START UP
REGISTER A
⑧ TRANSFER COMPLETION REPORT
② DATA SAVE
③ PARAMETER SAVE
④ PARAMETER RECOVERY
⑤ DATA RECOVERY
PROCESSOR #1
119
SCRIPT #0
SCRIPT #0 DATA
SCRIPT #1
SCRIPT #1 DATA
115
MEMORY #1
117
SCRIPT #N
SCRIPT #N DATA
CONTROL AREA
MEMORY #3

FIG.22

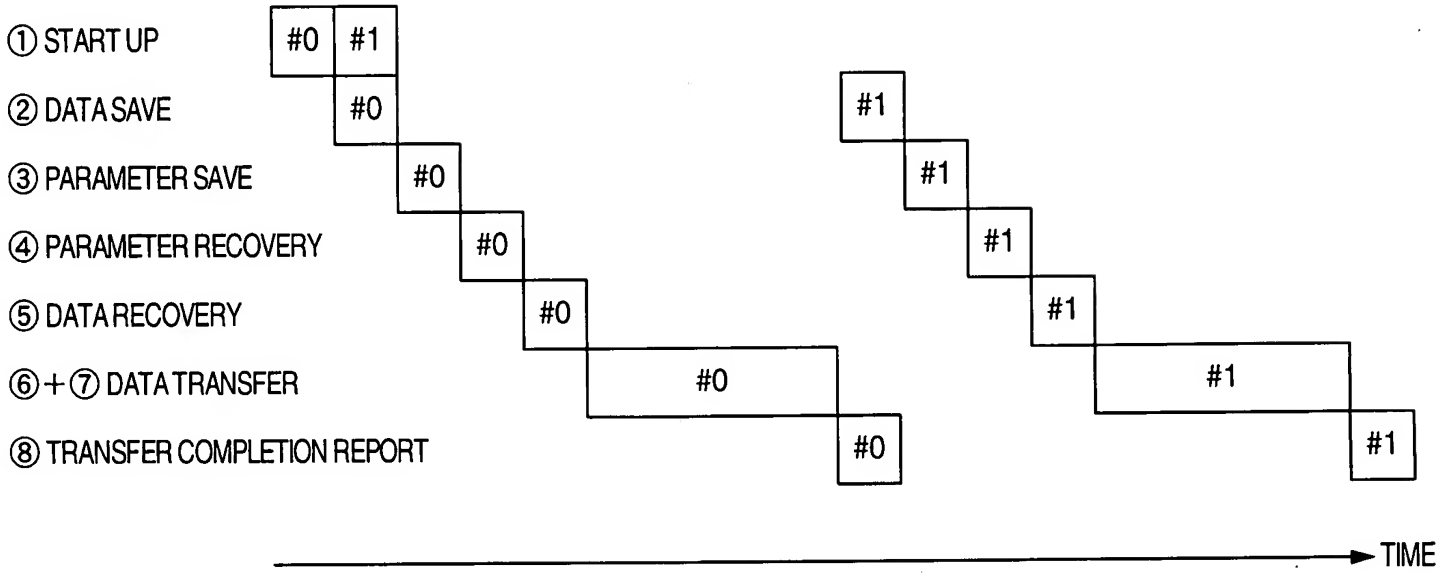

① START UP
② DATA SAVE
③ PARAMETER SAVE
④ PARAMETER RECOVERY
⑤ DATA RECOVERY
⑥+⑦ DATA TRANSFER
⑧ TRANSFER COMPLETION REPORT
#0
#1
TIME

FIG.23

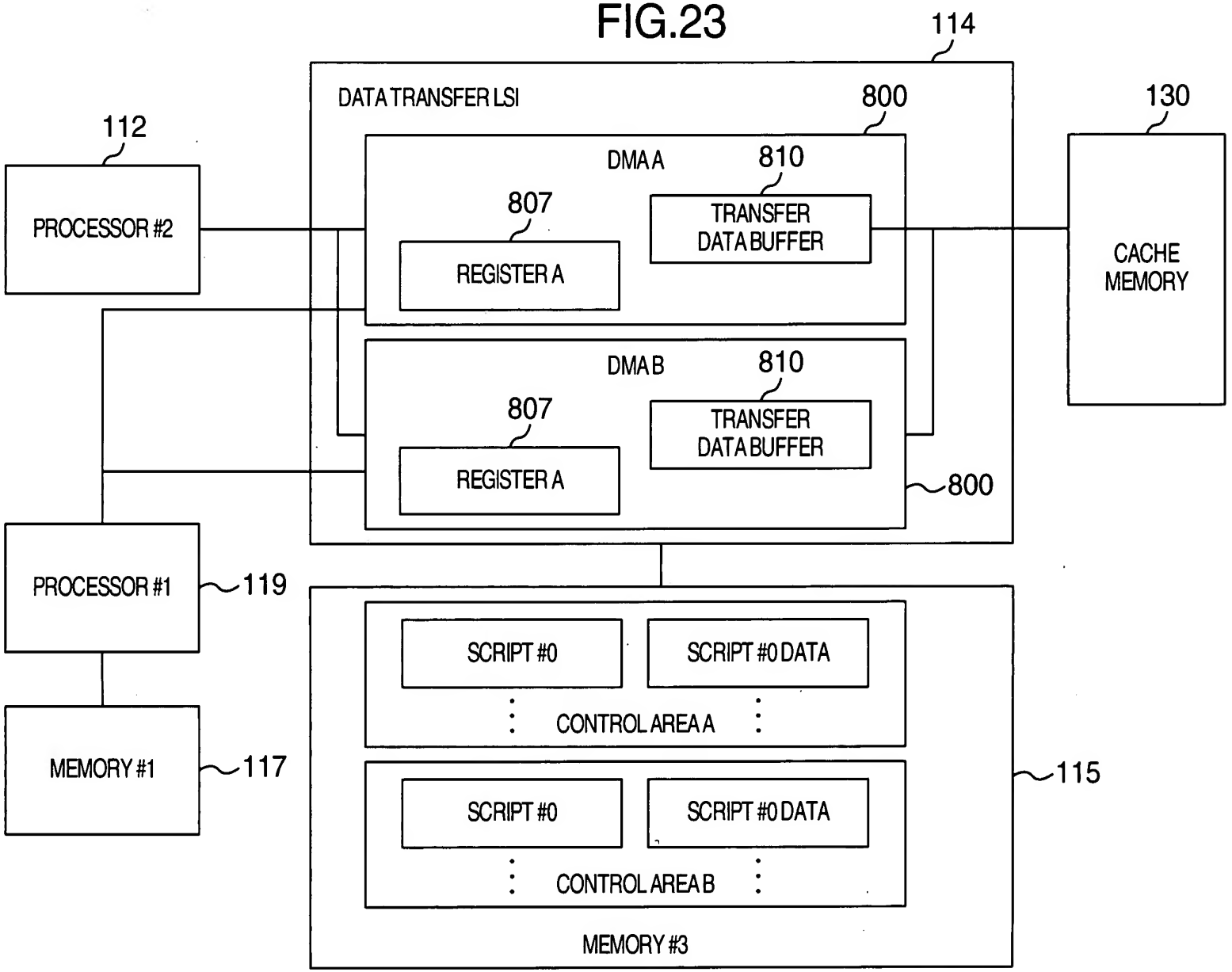

114
DATA TRANSFER LSI
800
130
112
DMA A
810
807
PROCESSOR #2
TRANSFER DATA BUFFER
REGISTER A
CACHE MEMORY
DMA B
810
807
TRANSFER DATA BUFFER
REGISTER A
800
PROCESSOR #1
119
SCRIPT #0
SCRIPT #0 DATA
CONTROL AREA A
MEMORY #1
117
115
SCRIPT #0
SCRIPT #0 DATA
CONTROL AREA B
MEMORY #3

FIG.24

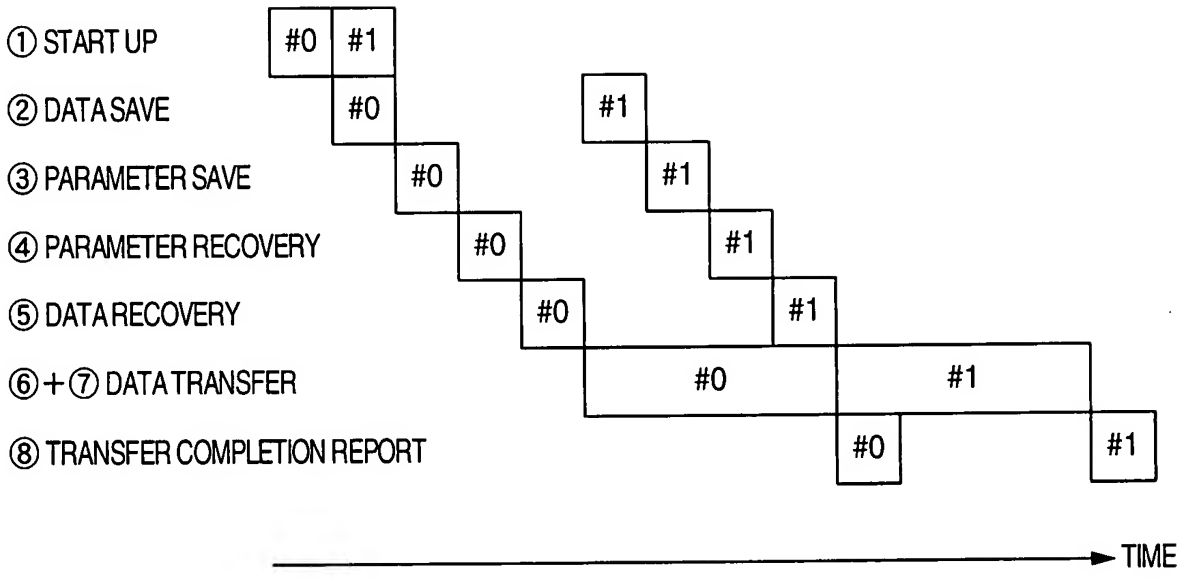

① START UP
② DATA SAVE
③ PARAMETER SAVE
④ PARAMETER RECOVERY
⑤ DATA RECOVERY
⑥+⑦ DATA TRANSFER
⑧ TRANSFER COMPLETION REPORT
#0
#1
TIME

FIG.25

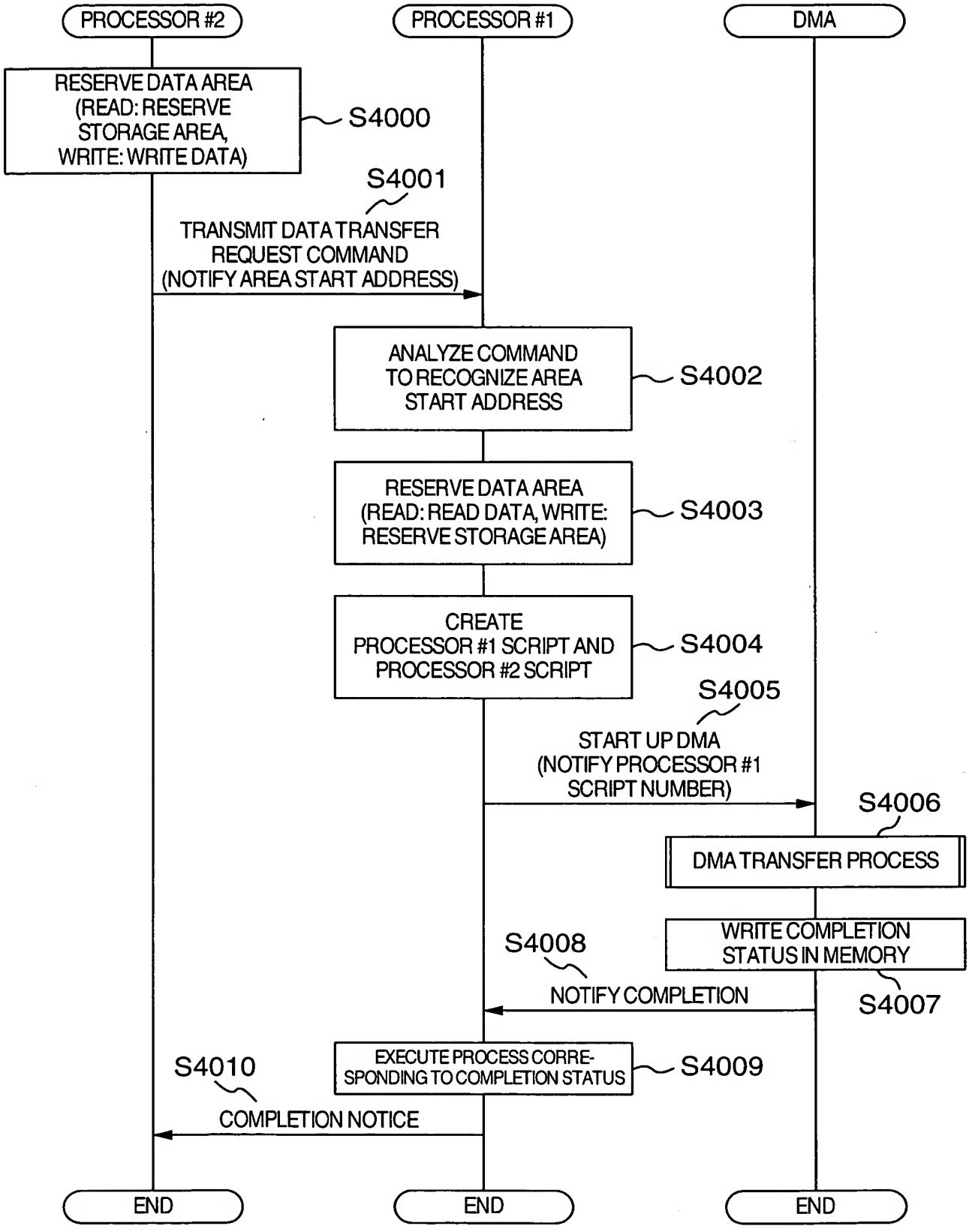

PROCESSOR #2
PROCESSOR #1
DMA
RESERVE DATA AREA (READ: RESERVE STORAGE AREA, WRITE: WRITE DATA)
S4000
S4001
TRANSMIT DATA TRANSFER REQUEST COMMAND (NOTIFY AREA START ADDRESS)
ANALYZE COMMAND TO RECOGNIZE AREA START ADDRESS
S4002
RESERVE DATA AREA (READ: READ DATA, WRITE: RESERVE STORAGE AREA)
S4003
CREATE PROCESSOR #1 SCRIPT AND PROCESSOR #2 SCRIPT
S4004
S4005
START UP DMA (NOTIFY PROCESSOR #1 SCRIPT NUMBER)
S4006
DMA TRANSFER PROCESS
WRITE COMPLETION STATUS IN MEMORY
S4007
S4008
NOTIFY COMPLETION
EXECUTE PROCESS CORRESPONDING TO COMPLETION STATUS
S4009
S4010
COMPLETION NOTICE
END
END
END

FIG.26

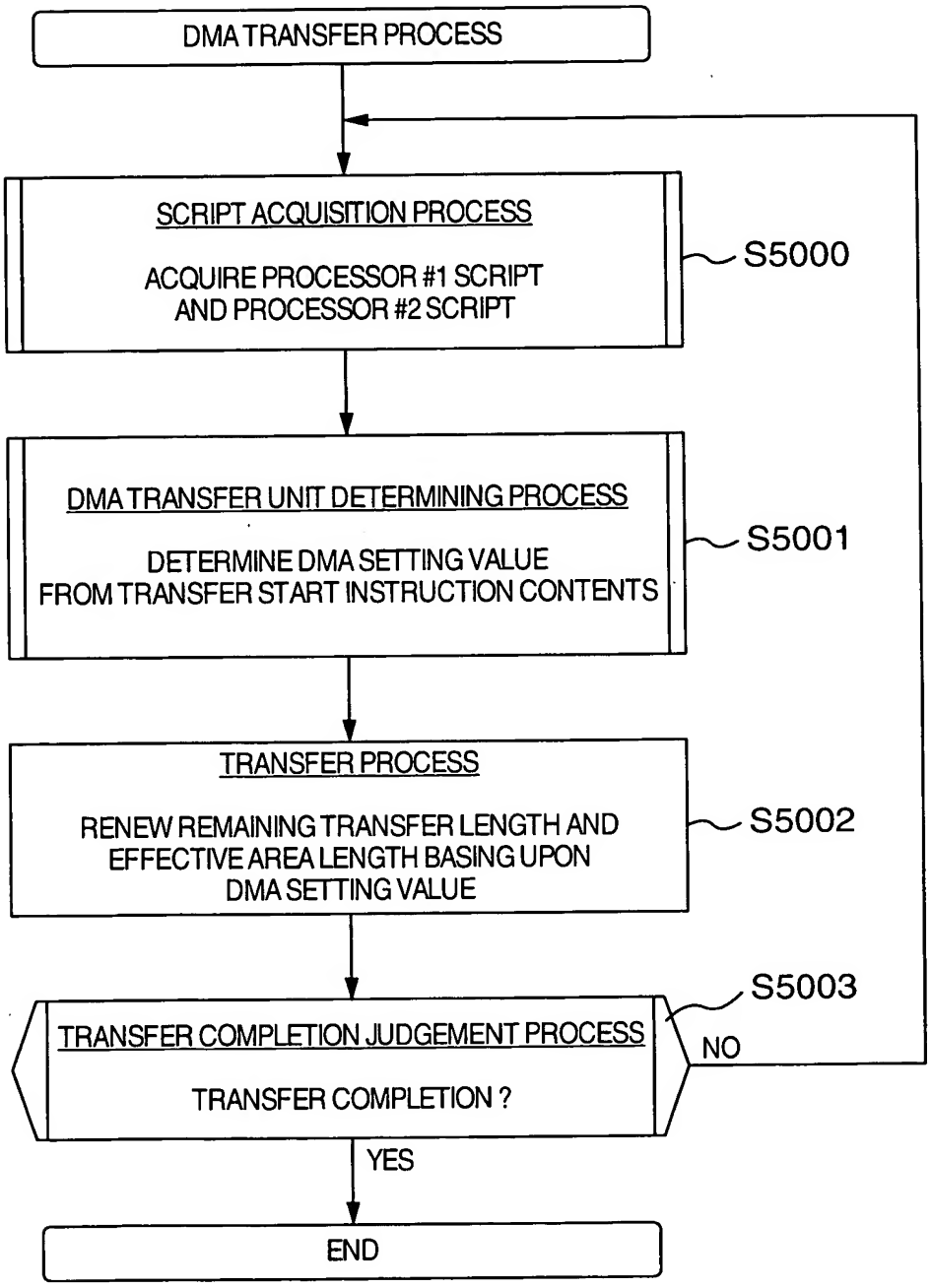

DMA TRANSFER PROCESS
SCRIPT ACQUISITION PROCESS
ACQUIRE PROCESSOR #1 SCRIPT AND PROCESSOR #2 SCRIPT
S5000
DMA TRANSFER UNIT DETERMINING PROCESS
DETERMINE DMA SETTING VALUE FROM TRANSFER START INSTRUCTION CONTENTS
S5001
TRANSFER PROCESS
RENEW REMAINING TRANSFER LENGTH AND EFFECTIVE AREA LENGTH BASING UPON DMA SETTING VALUE
S5002
S5003
TRANSFER COMPLETION JUDGEMENT PROCESS
TRANSFER COMPLETION ?
NO
YES
END

FIG.27

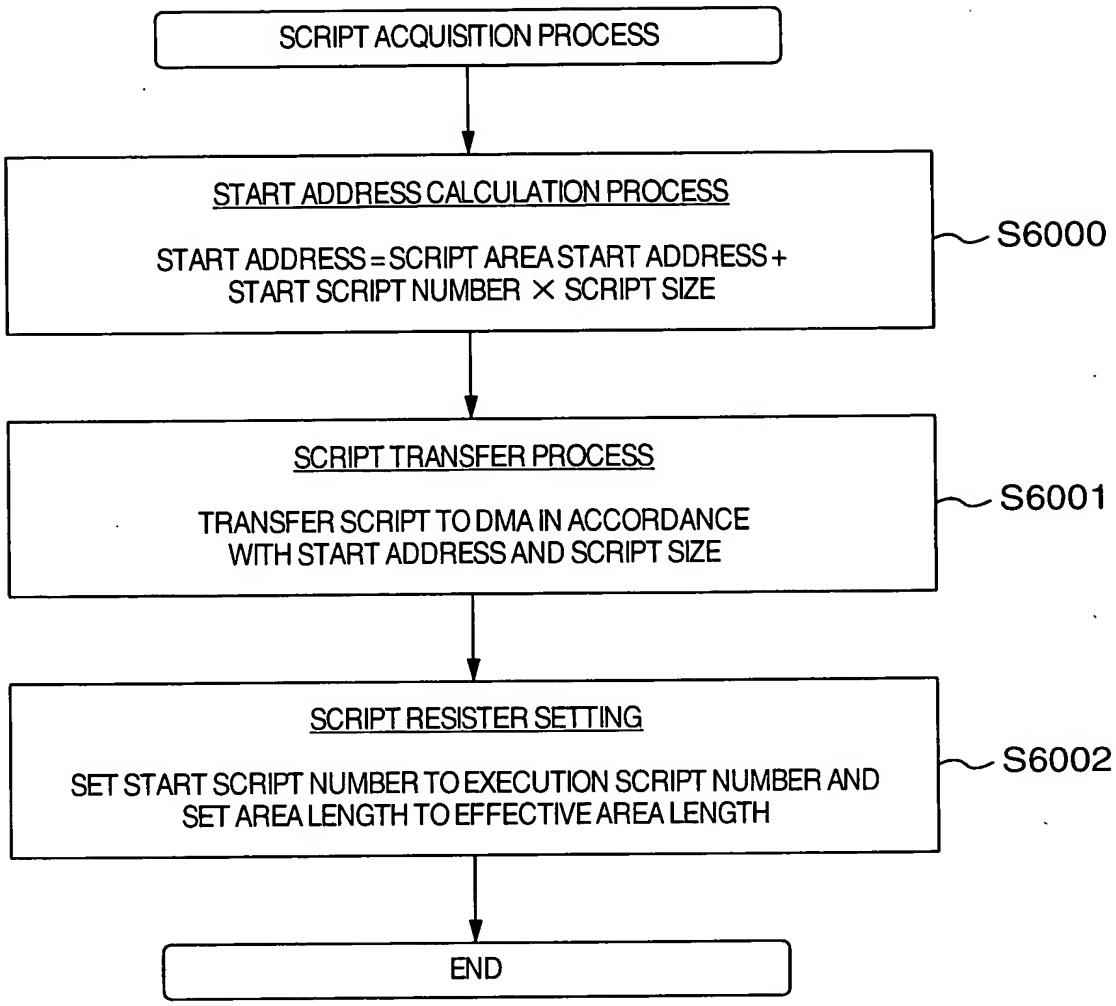

SCRIPT ACQUISITION PROCESS
START ADDRESS CALCULATION PROCESS
START ADDRESS = SCRIPT AREA START ADDRESS + START SCRIPT NUMBER × SCRIPT SIZE
S6000
SCRIPT TRANSFER PROCESS
TRANSFER SCRIPT TO DMA IN ACCORDANCE WITH START ADDRESS AND SCRIPT SIZE
S6001
SCRIPT RESISTER SETTING
SET START SCRIPT NUMBER TO EXECUTION SCRIPT NUMBER AND SET AREA LENGTH TO EFFECTIVE AREA LENGTH
S6002
END

FIG.28

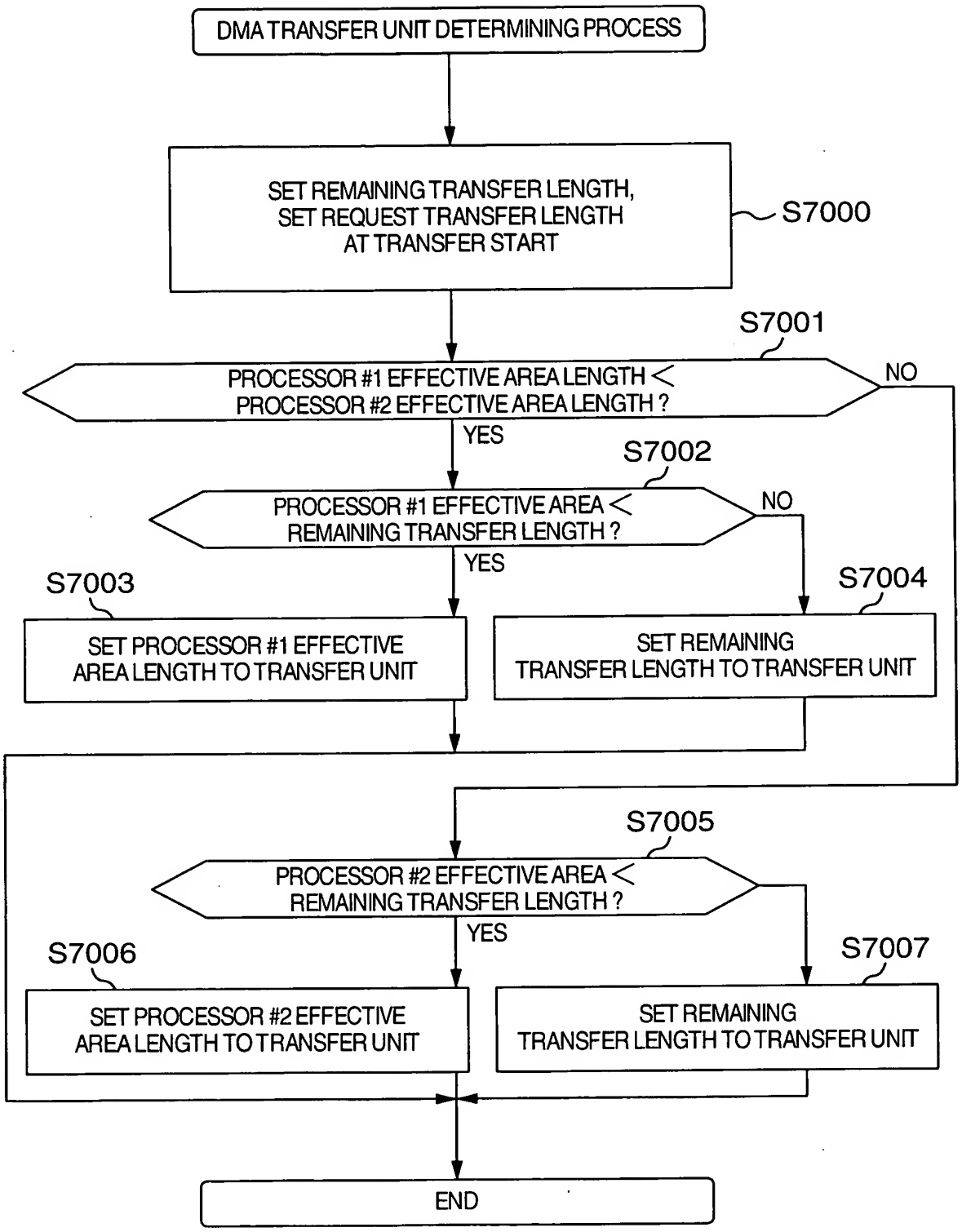

DMA TRANSFER UNIT DETERMINING PROCESS
SET REMAINING TRANSFER LENGTH, SET REQUEST TRANSFER LENGTH AT TRANSFER START
S7000
S7001
PROCESSOR #1 EFFECTIVE AREA LENGTH < PROCESSOR #2 EFFECTIVE AREA LENGTH ?
NO
YES
S7002
PROCESSOR #1 EFFECTIVE AREA < REMAINING TRANSFER LENGTH ?
NO
YES
S7003
SET PROCESSOR #1 EFFECTIVE AREA LENGTH TO TRANSFER UNIT
S7004
SET REMAINING TRANSFER LENGTH TO TRANSFER UNIT
S7005
PROCESSOR #2 EFFECTIVE AREA < REMAINING TRANSFER LENGTH ?
YES
S7006
SET PROCESSOR #2 EFFECTIVE AREA LENGTH TO TRANSFER UNIT
S7007
SET REMAINING TRANSFER LENGTH TO TRANSFER UNIT
END

FIG.29

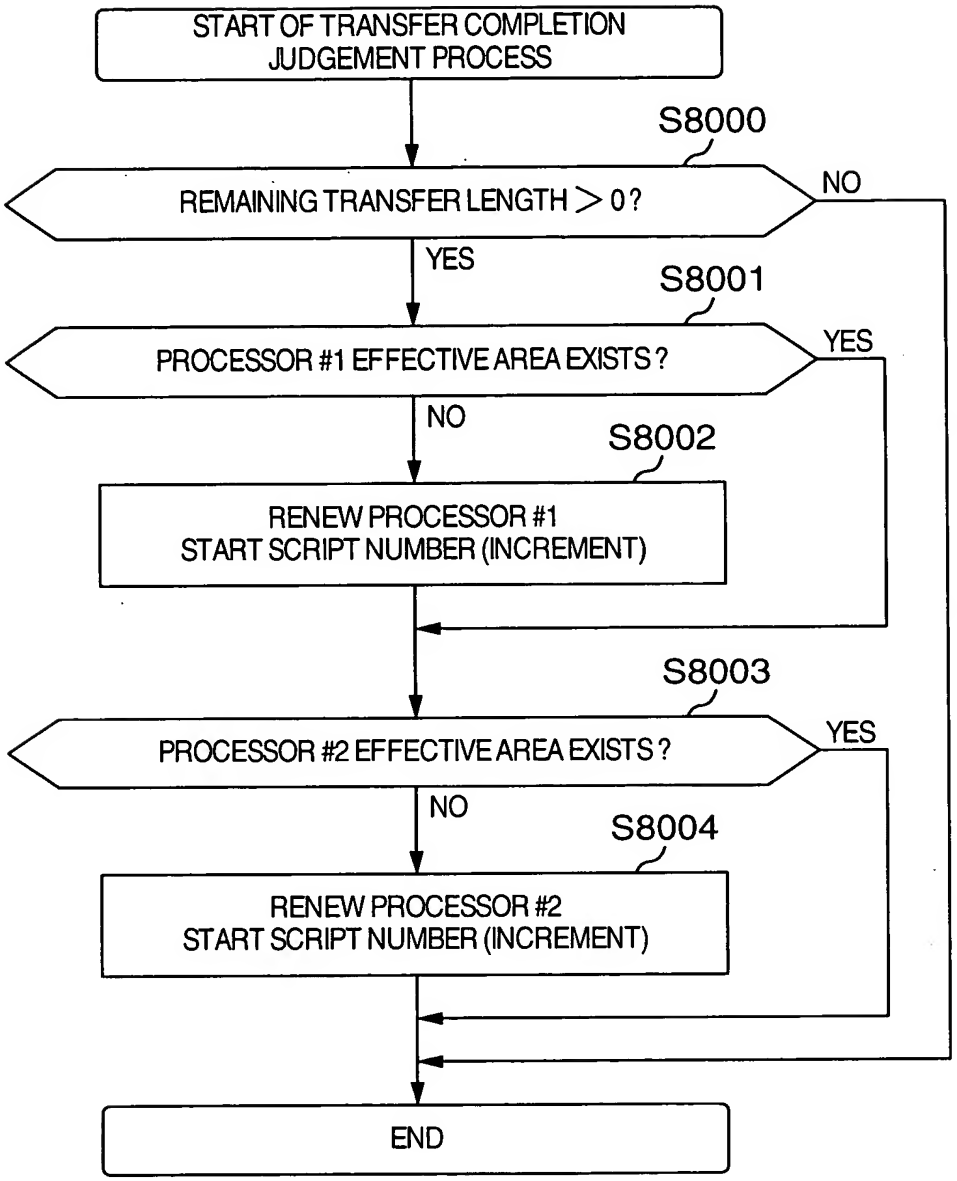

START OF TRANSFER COMPLETION JUDGEMENT PROCESS
S8000
REMAINING TRANSFER LENGTH > 0 ?
NO
YES
S8001
PROCESSOR #1 EFFECTIVE AREA EXISTS ?
YES
NO
S8002
RENEW PROCESSOR #1 START SCRIPT NUMBER (INCREMENT)
S8003
PROCESSOR #2 EFFECTIVE AREA EXISTS ?
YES
NO
S8004
RENEW PROCESSOR #2 START SCRIPT NUMBER (INCREMENT)
END

FIG.30

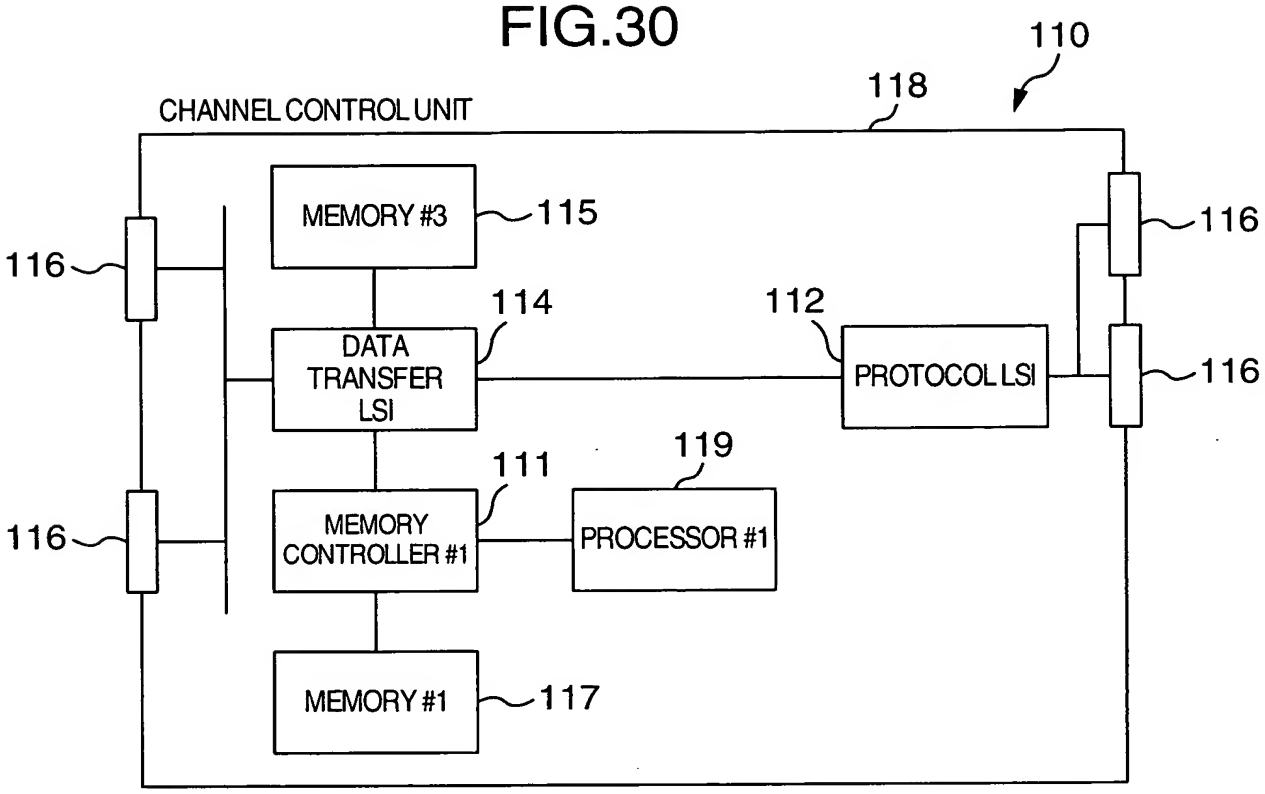

110
118
CHANNEL CONTROL UNIT
MEMORY #3
115
116
116
114
112
DATA TRANSFER LSI
PROTOCOL LSI
116
119
111
116
MEMORY CONTROLLER #1
PROCESSOR #1
MEMORY #1
117

FIG.31

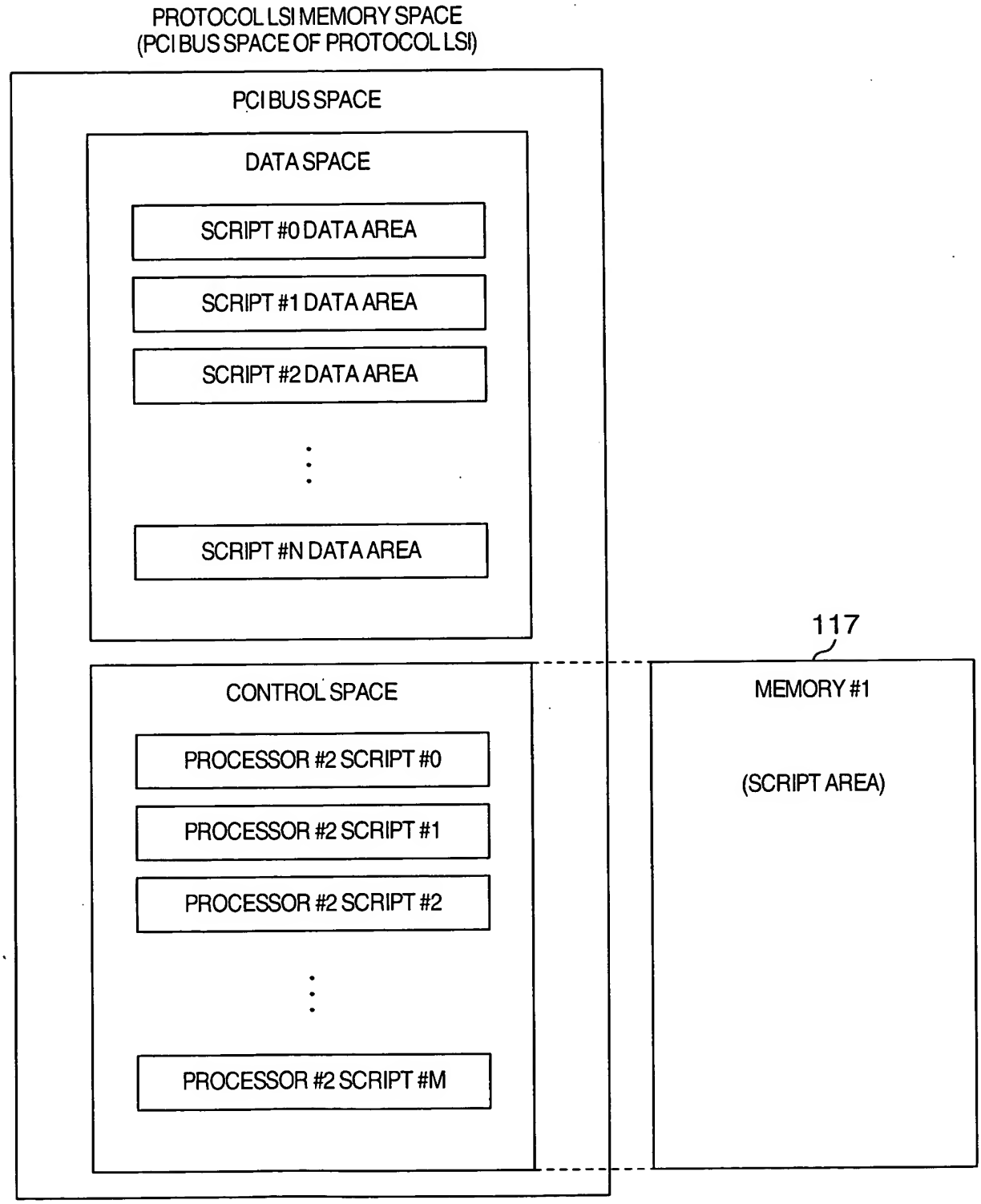
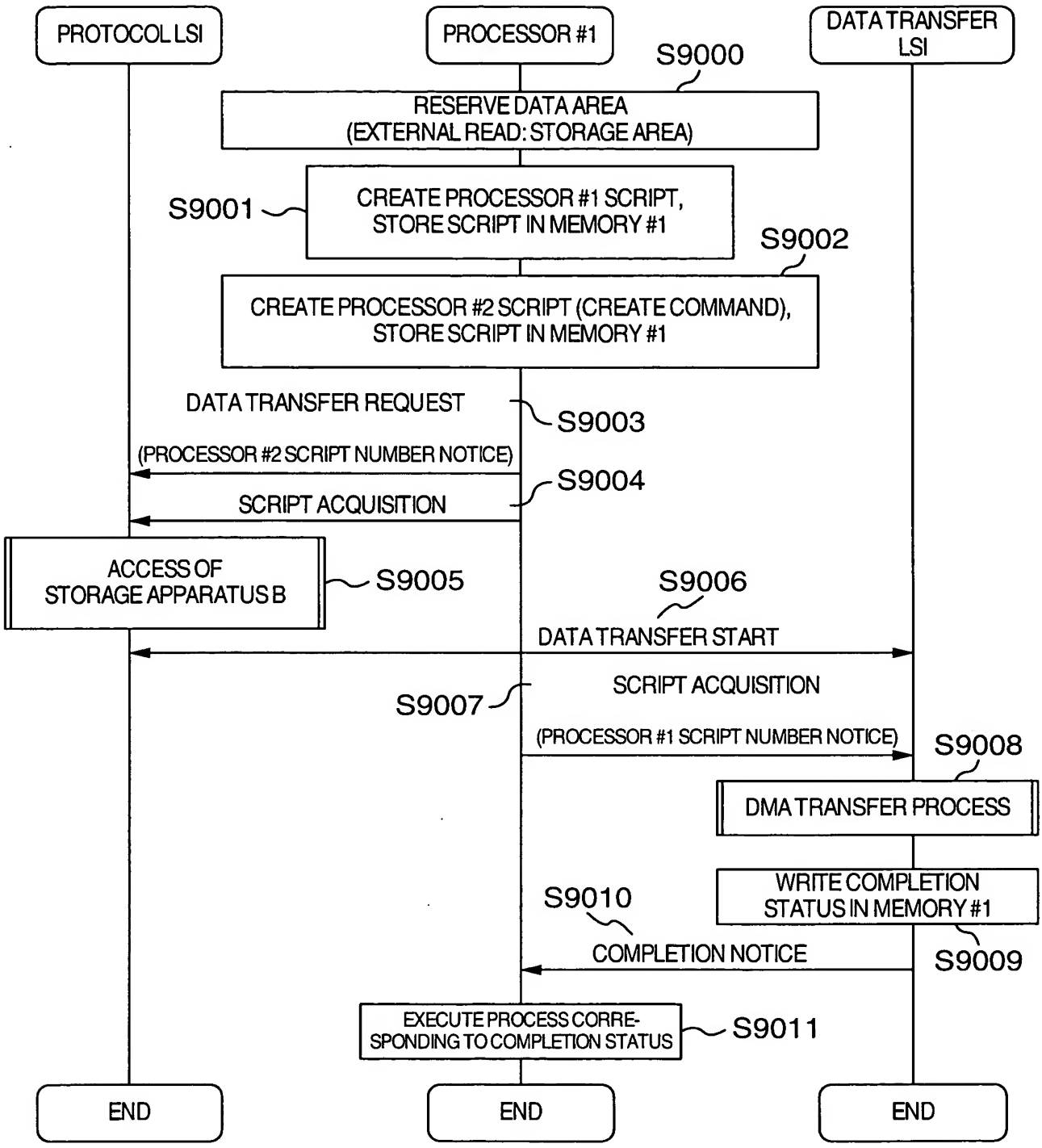

PROTOCOL LSI MEMORY SPACE
(PCI BUS SPACE OF PROTOCOL LSI)
PCI BUS SPACE
DATA SPACE
SCRIPT #0 DATA AREA
SCRIPT #1 DATA AREA
SCRIPT #2 DATA AREA
SCRIPT #N DATA AREA
CONTROL SPACE
PROCESSOR #2 SCRIPT #0
PROCESSOR #2 SCRIPT #1
PROCESSOR #2 SCRIPT #2
PROCESSOR #2 SCRIPT #M
117
MEMORY #1
(SCRIPT AREA)

FIG.32


PROTOCOL LSI
PROCESSOR #1
DATA TRANSFER LSI
S9000
RESERVE DATA AREA (EXTERNAL READ: STORAGE AREA)
S9001
CREATE PROCESSOR #1 SCRIPT, STORE SCRIPT IN MEMORY #1
S9002
CREATE PROCESSOR #2 SCRIPT (CREATE COMMAND), STORE SCRIPT IN MEMORY #1
DATA TRANSFER REQUEST
S9003
(PROCESSOR #2 SCRIPT NUMBER NOTICE)
S9004
SCRIPT ACQUISITION
ACCESS OF STORAGE APPARATUS B
S9005
S9006
DATA TRANSFER START
S9007
SCRIPT ACQUISITION
(PROCESSOR #1 SCRIPT NUMBER NOTICE)
S9008
DMA TRANSFER PROCESS
WRITE COMPLETION STATUS IN MEMORY #1
S9009
S9010
COMPLETION NOTICE
EXECUTE PROCESS CORRESPONDING TO COMPLETION STATUS
S9011
END
END
END